拥抱变革：基于模型的通信系统设计实践

中国空间技术研究院西安分院
主讲人：许鹏飞

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汇报内容

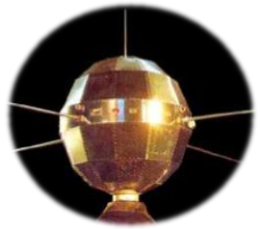
1 基本情况介绍

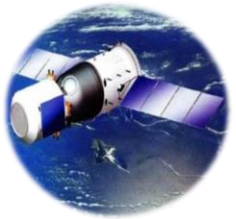
2 传统FPGA开发流程

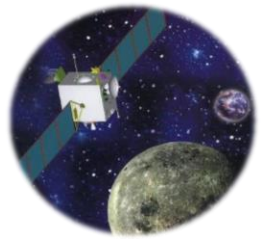
3 MATLAB解决方案

4 MATLAB应用实效

5 经验与总结







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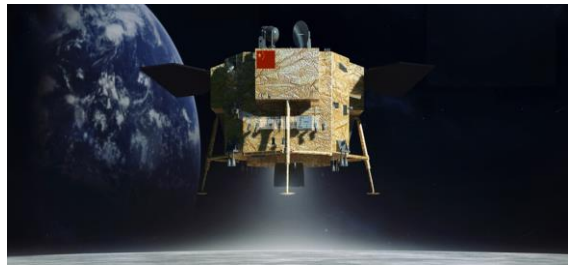
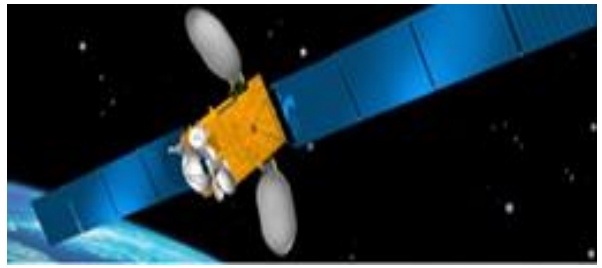
一、基本情况介绍

1 中国空间技术研究院西安分院简介

我国从事卫星有效载荷设计和空间电子设备研制的专业研究单位。

2 通信技术研究所简介

主要从事卫星通信系统论证设计及其核心产品研制。

3 演讲人

许鹏飞，高级工程师，主要研究方向为卫星通信等。

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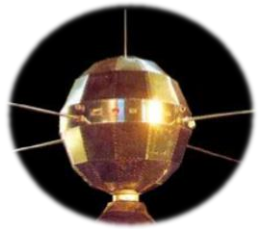
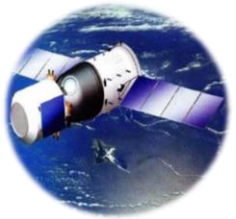
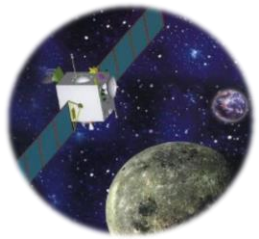

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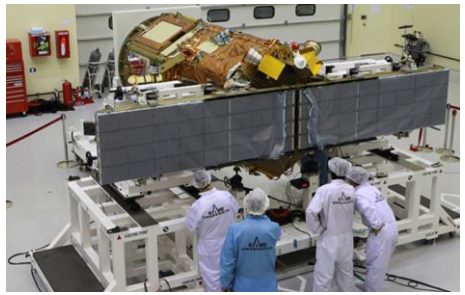
二、传统FPGA开发流程

1 传统开发流程

```
% Add reference to the API wrapper.
apiRoot = 'C:\Program Files\Audio Precision\APx500 2.4\Api\';
NET.addAssembly([apiRoot 'AudioPrecision.API2.dll'])

% Create an instance of the application, and make it visible (it doesn't
% have to be visible to work, it just lets us see what's happening).
apx = AudioPrecision.API.APx500_Application;
apx.Visible = true;

% Turn off the signal monitors.
apx.SignalMonitorsEnabled = false;

% Select the Frequency Response measurement.
apx.ShowMeasurement('Signal Path1', 'Frequency Response')

% Set the generator parameters. Matlab can only set a property on an
% explicit handle.
gen = apx.FrequencyResponse.Generator;
startFreq = gen.StartFrequency;
startFreq.Unit = 'Hz';
startFreq.Value = 30;
stopFreq = gen.StopFrequency;
stopFreq.Value = 18000;
levels = gen.AnalogLevels;
levels.Unit = 'Vrms';
levels.SetValue(AudioPrecision.API.OutputChannelIndex.Ch1, 1.5);

% Start the measurement. Success is true if the measurement worked.
```

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY TestBench IS
END TestBench;
ARCHITECTURE TestBenchArch OF TestBench IS
   COMPONENT UnitUnderTest IS
      PORT (a, b: IN std_logic;
            c: OUT std_logic);
   END COMPONENT;
   SIGNAL x, y, z: std_logic;
BEGIN
   CompToTest: UnitUnderTest PORT MAP (x, y, z);
   PROCESS
   BEGIN
      x <= '0'; y <= '1';
      WAIT FOR 5 ns;
      x <= '1';
      WAIT FOR 25 ns;
      x <= '0'; y <= '0';
      WAIT FOR 10 ns;
      x <= '1';
      WAIT FOR 20 ns;
      x <= '0'; y <= '1';
      WAIT FOR 5 ns;
   END PROCESS;
END TestBenchArch;
```



1.需求和技术指标 → 2.设计 → 3.实现 → 4.测试和验证

文本文档

算法级系统设计

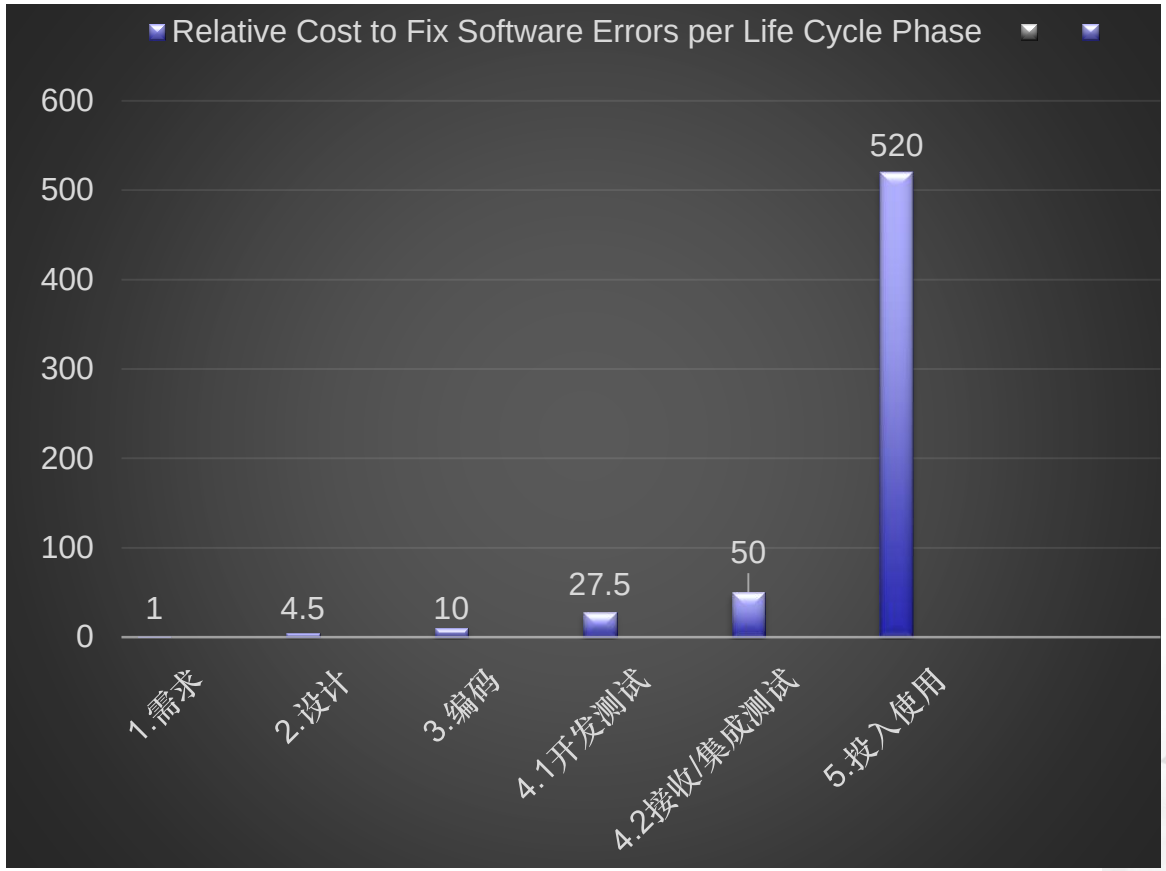
手工HDL编码

传统测试

二、传统FPGA开发流程

2 纠错成本高

Error Cost Escalation Through the Project Life Cycle – NASA



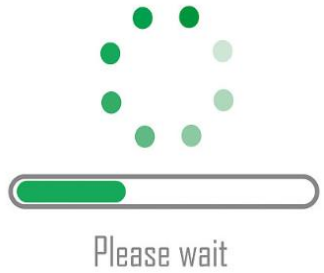
二、传统FPGA开发流程

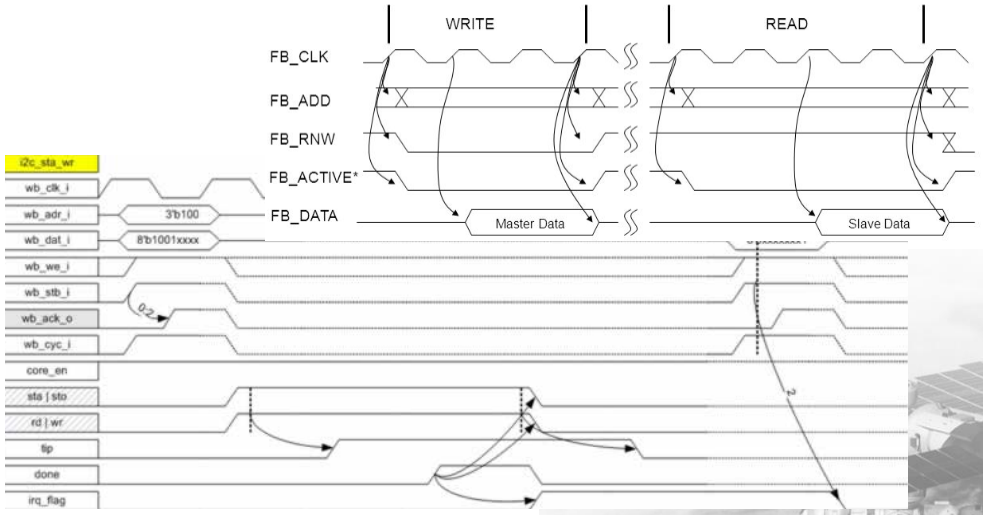
3 开发效率低

- 设计抽象级低

RTL HDL

- 迭代更新慢





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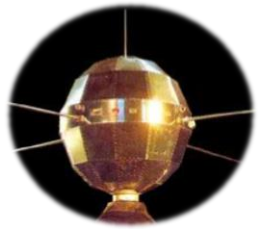
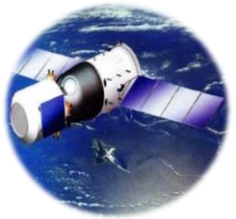
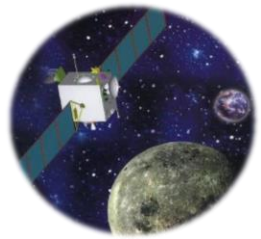
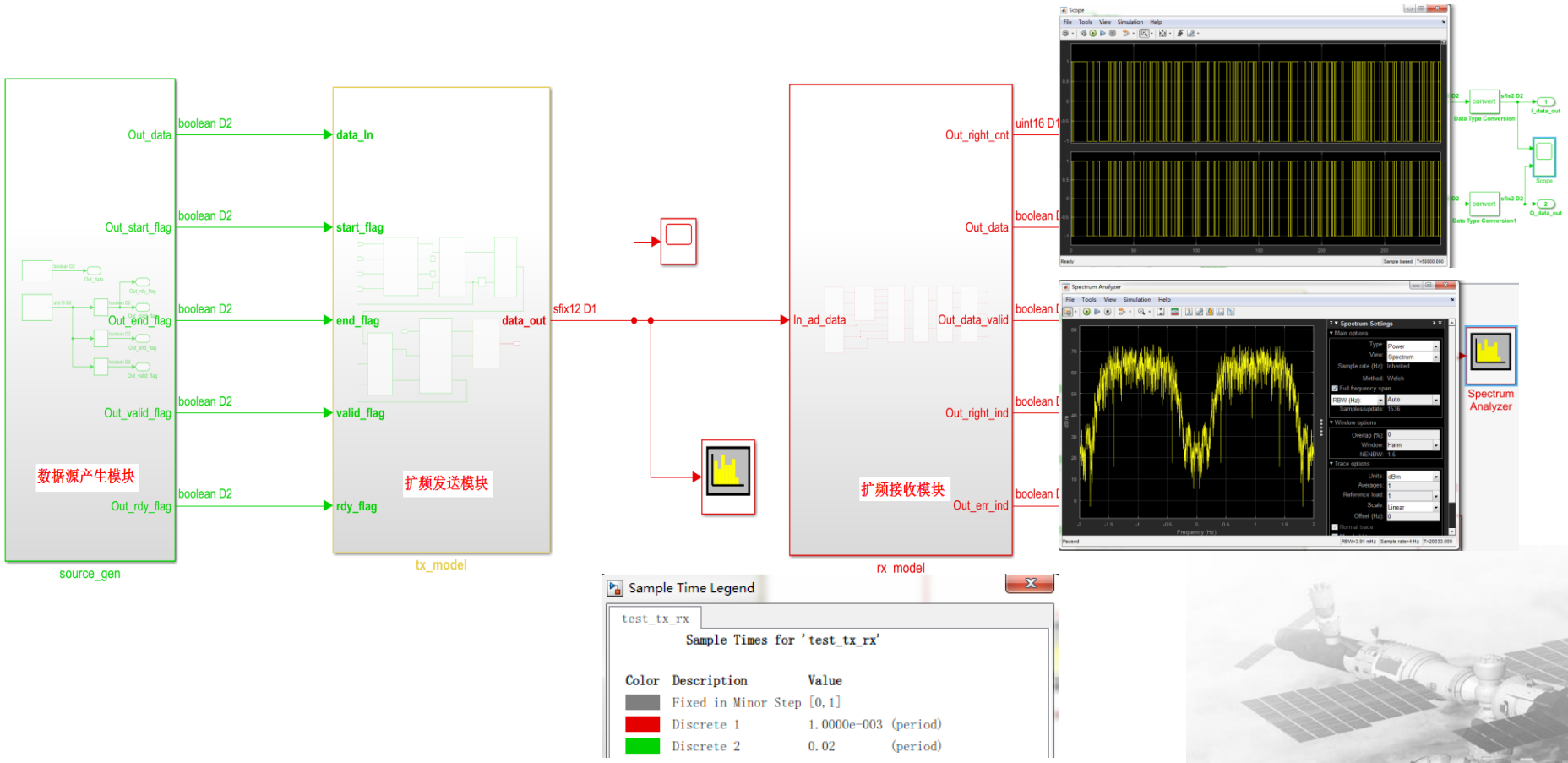




三、MATLAB解决方案

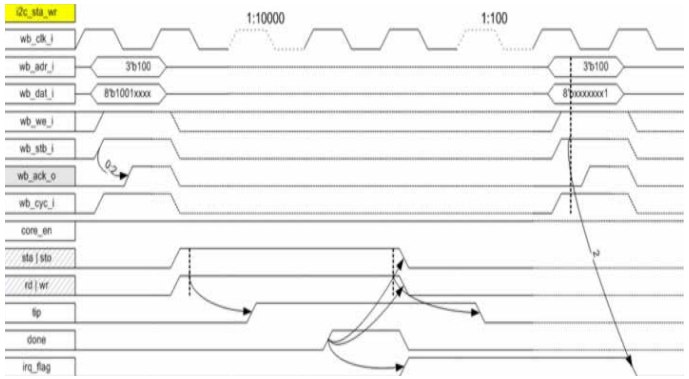
1 需求分析

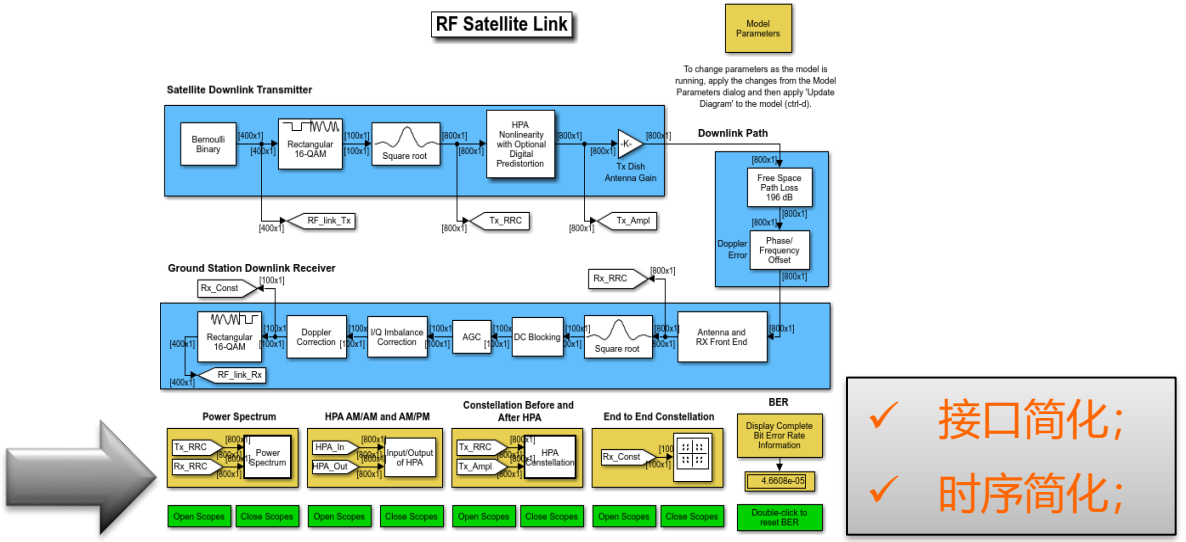


三、 MATLAB解决方案

2 设计

➢ 抽象级提高





- ✓ 接口简化；
- ✓ 时序简化；

- ➢ **建模对象：** 门电路比特级信号

定点数、复数、向量、矩阵

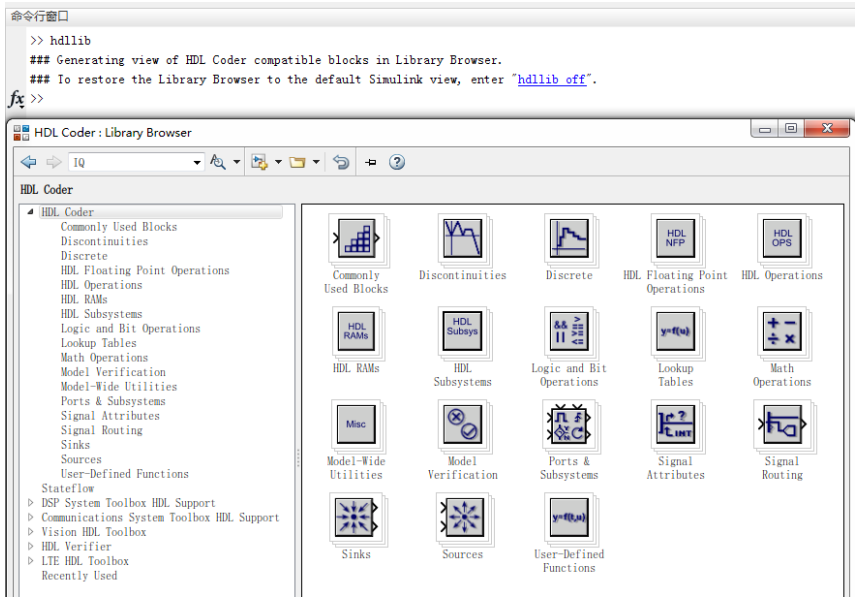
- ➢ **行　　为：** 加减乘，与或非；同/异步时序；

算法级行为

三、 MATLAB解决方案

2 设计

➢ 模块库支持

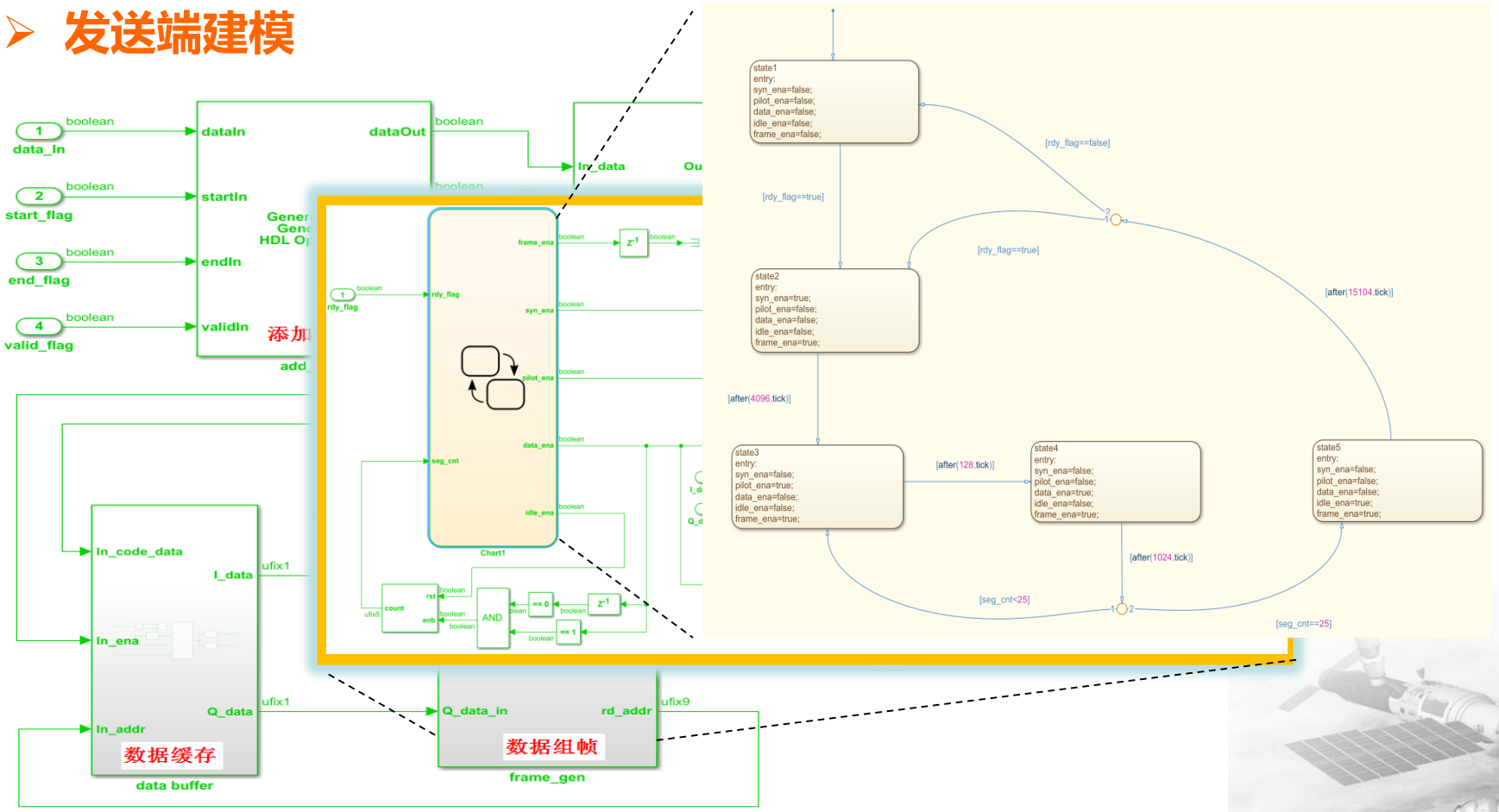


序号	模块类型	模块
1	存储模块	Dual Port RAM、Dual Rate Dual Port RAM、FIFO、Simple Dual Port RAM、Simple Port RAM、Lookup Table（ROM）
2	三角函数模块	Sine/Cosine、NCO
3	滤波模块	Biquad Filter、Channelizer HDL Optimized、CIC Decimation/Interpolation、FIR filter、FIR Decimation/Interpolation、LMS Filter、Raised Cosine Receive/ Transmit Filter
4	FFT	FFT/IFFT
5	编译码模块	RS编译码、卷积码编译码、CRC校验
6	交织模块	Convolutional Interleaver/Deinterleaver、General Multiplexed Interleaver/Deinterleaver
7	调制模块	BPSK、QPSK、M-PSK Modulator/Demodulator、Rectangular QAM Modulator/ Demodulator
8	支持LTE标准的相关模块	Convolutional Interleaver/Deinterleaver、CRC Encoder/Decoder、Turbo Encoder/Decoder

三、 MATLAB解决方案

2 设计

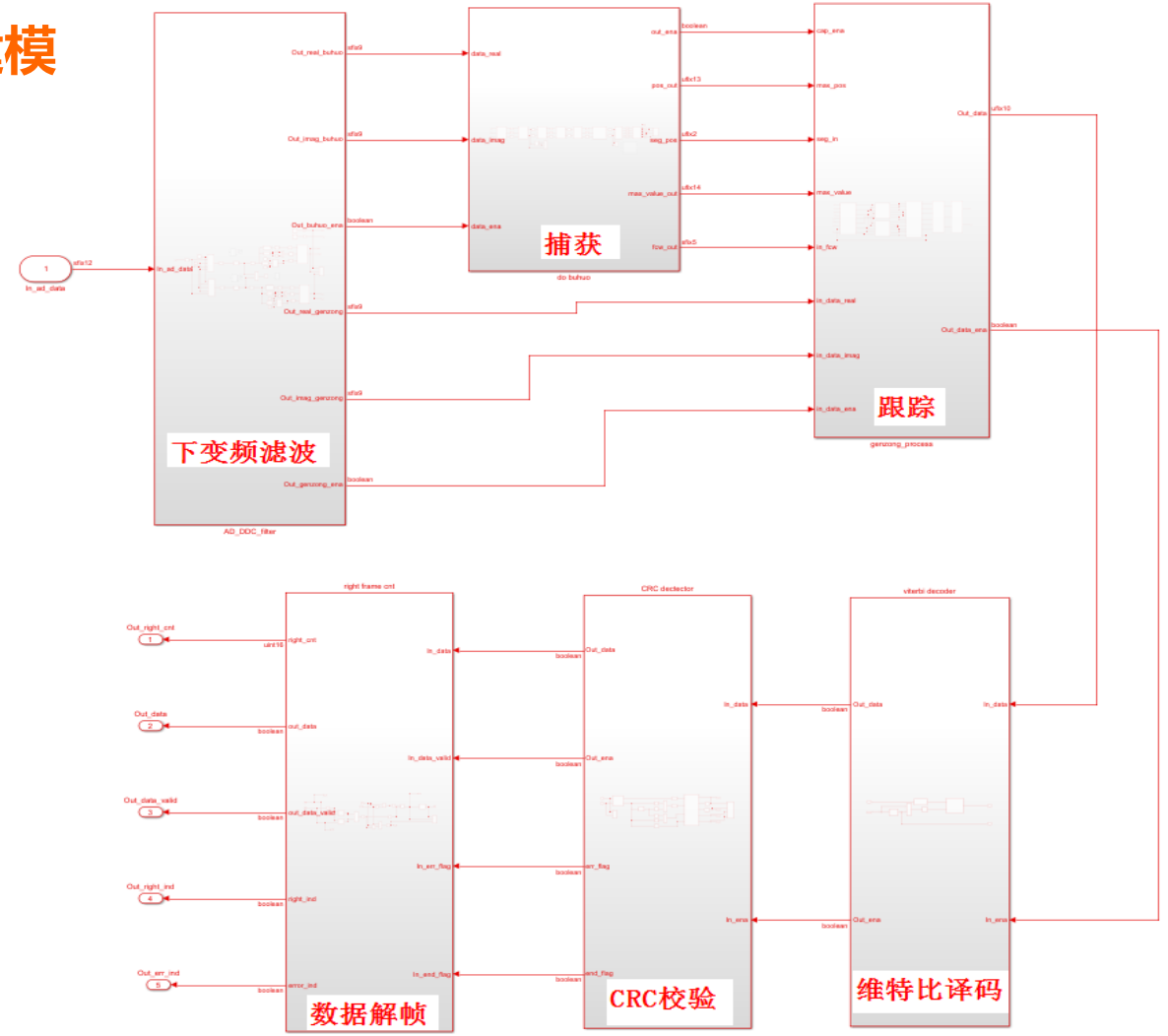
➢ 发送端建模



三、 MATLAB解决方案

2 设计

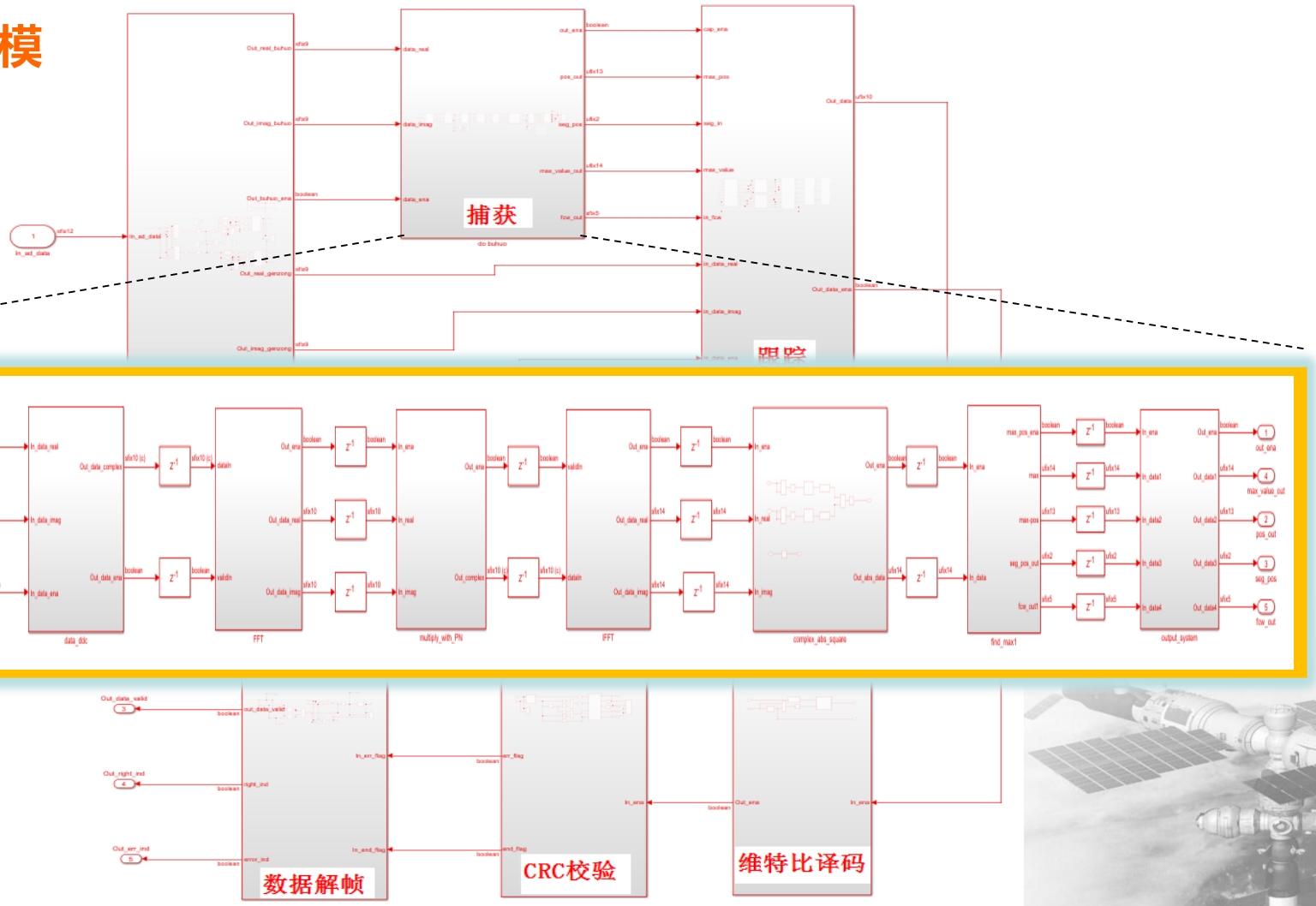
- **接收端建模**



三、 MATLAB解决方案

2 设计

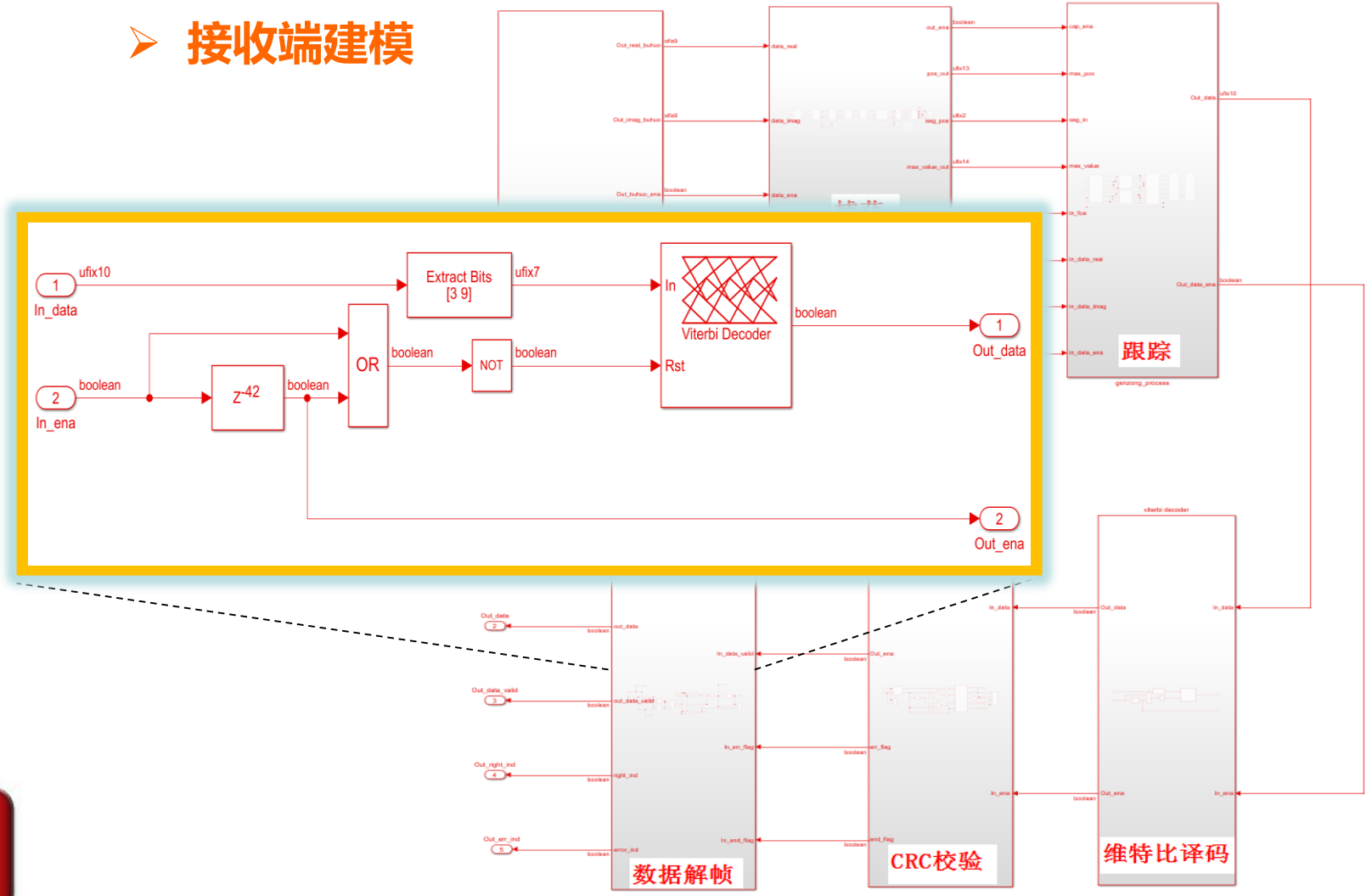
➢ 接收端建模



三、 MATLAB解决方案

2 设计

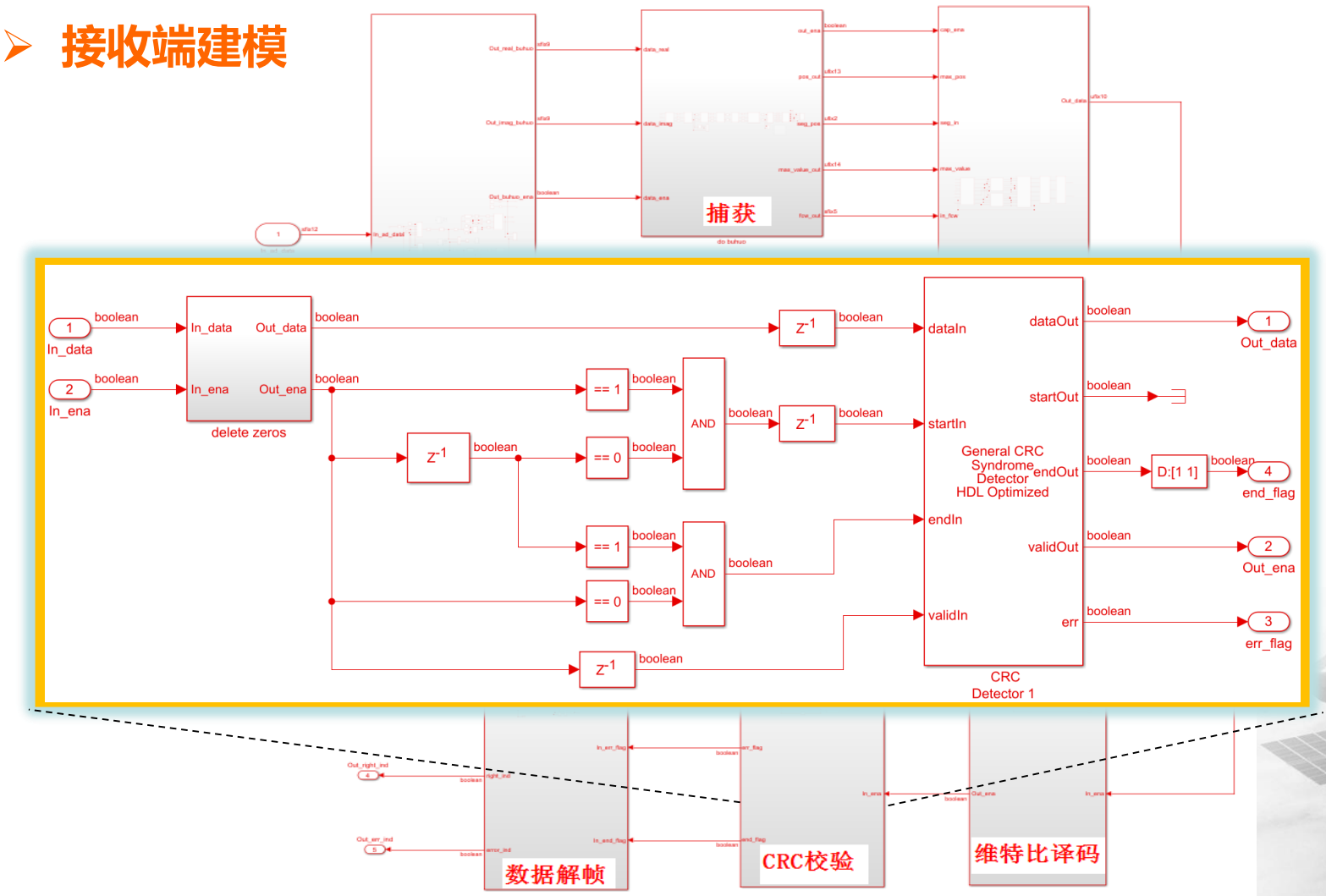
➢ 接收端建模



三、 MATLAB解决方案

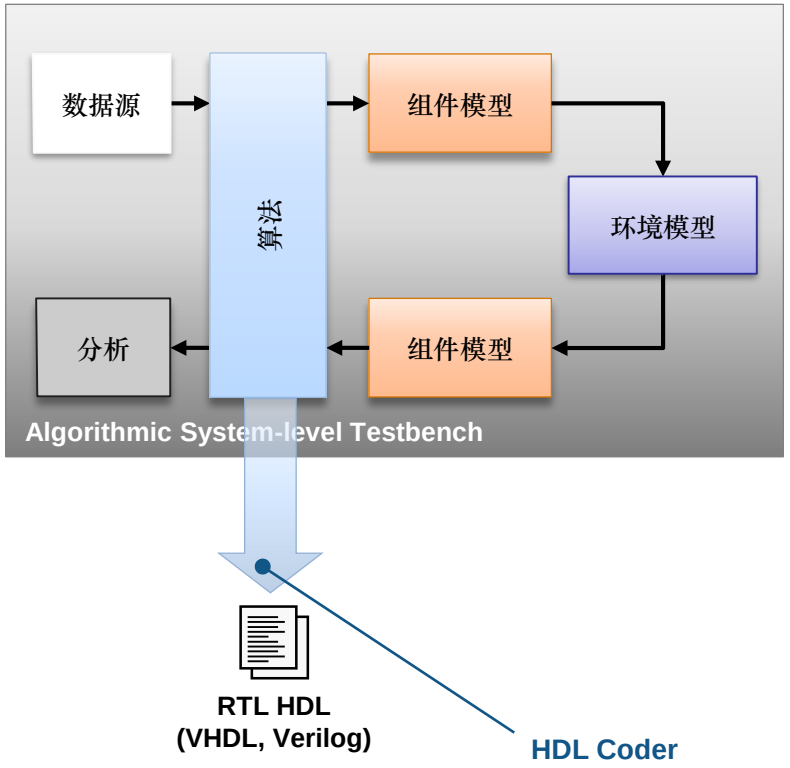
2 设计

➢ 接收端建模

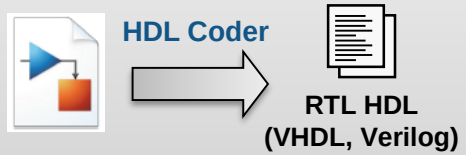


三、 MATLAB解决方案

3 实现



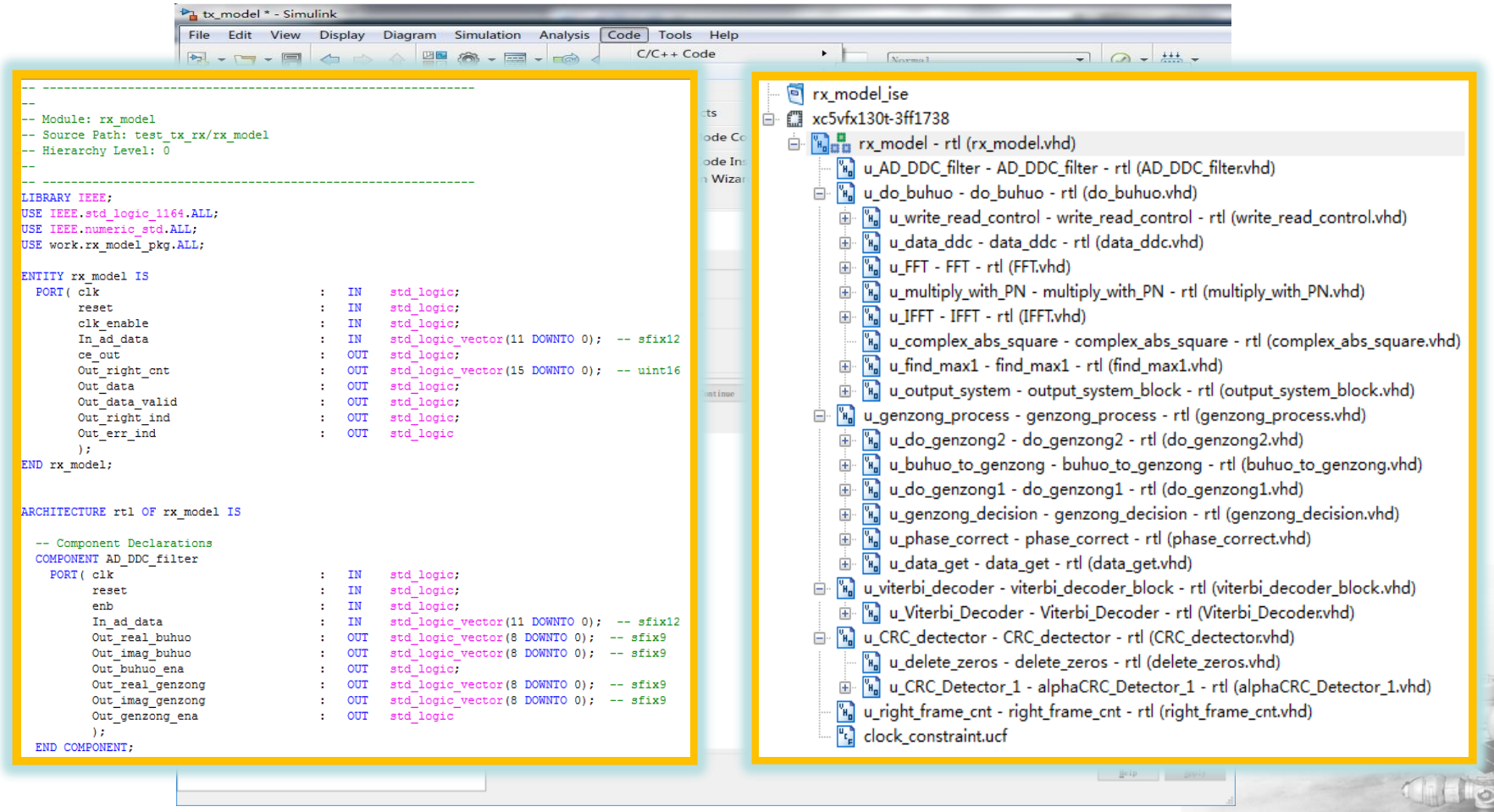
✓ 时序自动设计；



✓ 快速迭代；

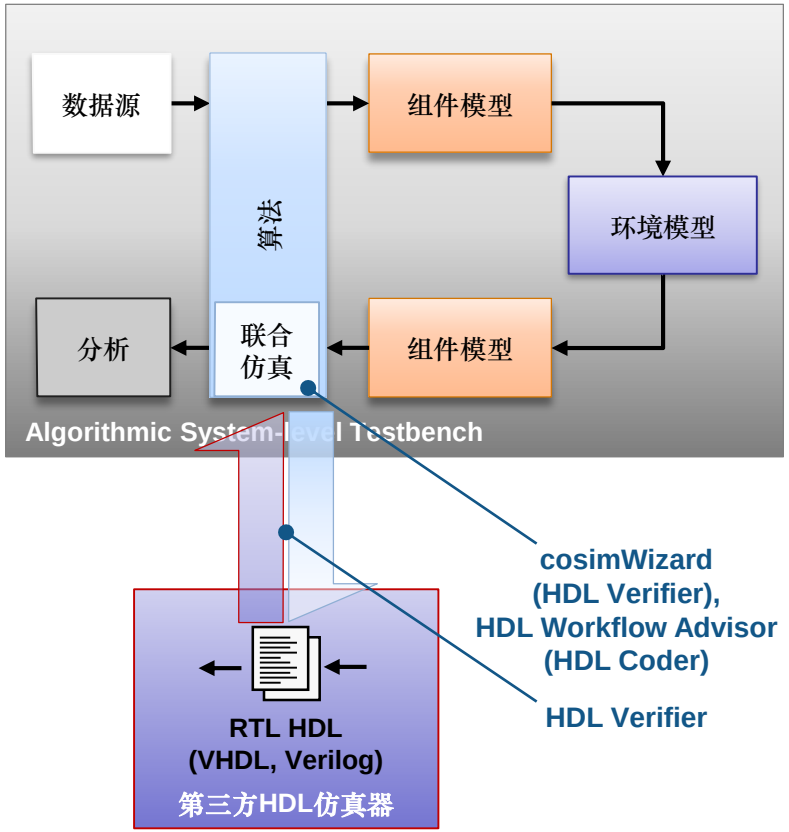
三、 MATLAB解决方案

3 实现（自动生成代码）



三、 MATLAB解决方案

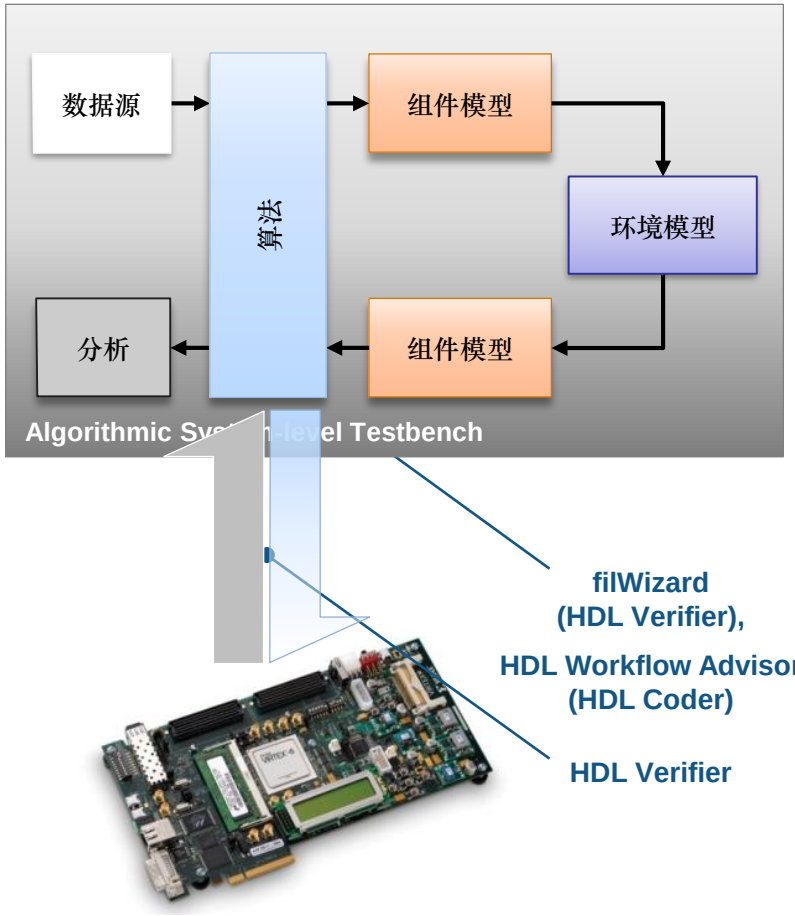
4 测试与验证



✓ 自动生成Testbench，联合仿真

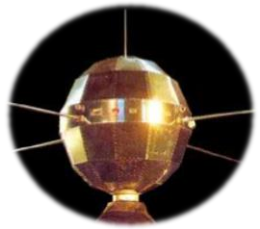
三、 MATLAB解决方案

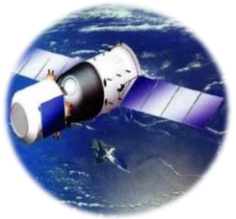
4 测试与验证

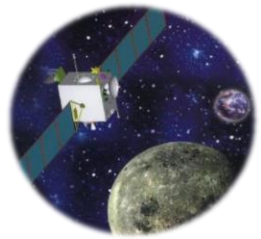


✓ 自动生成Testbench, FPGA硬件在环

汇报内容

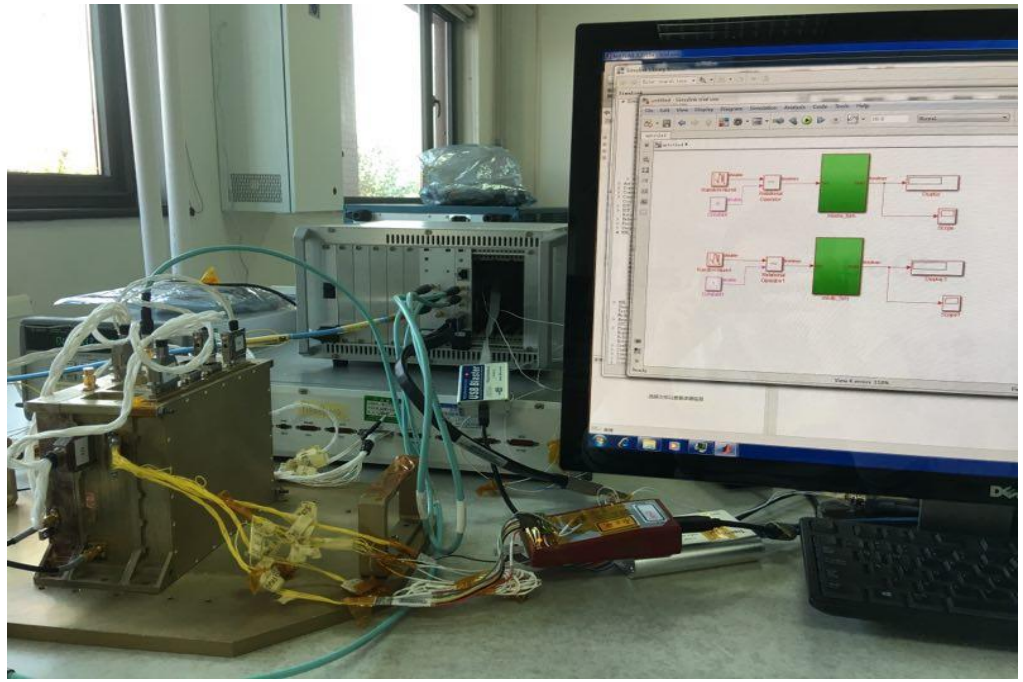






四、MATLAB应用实效

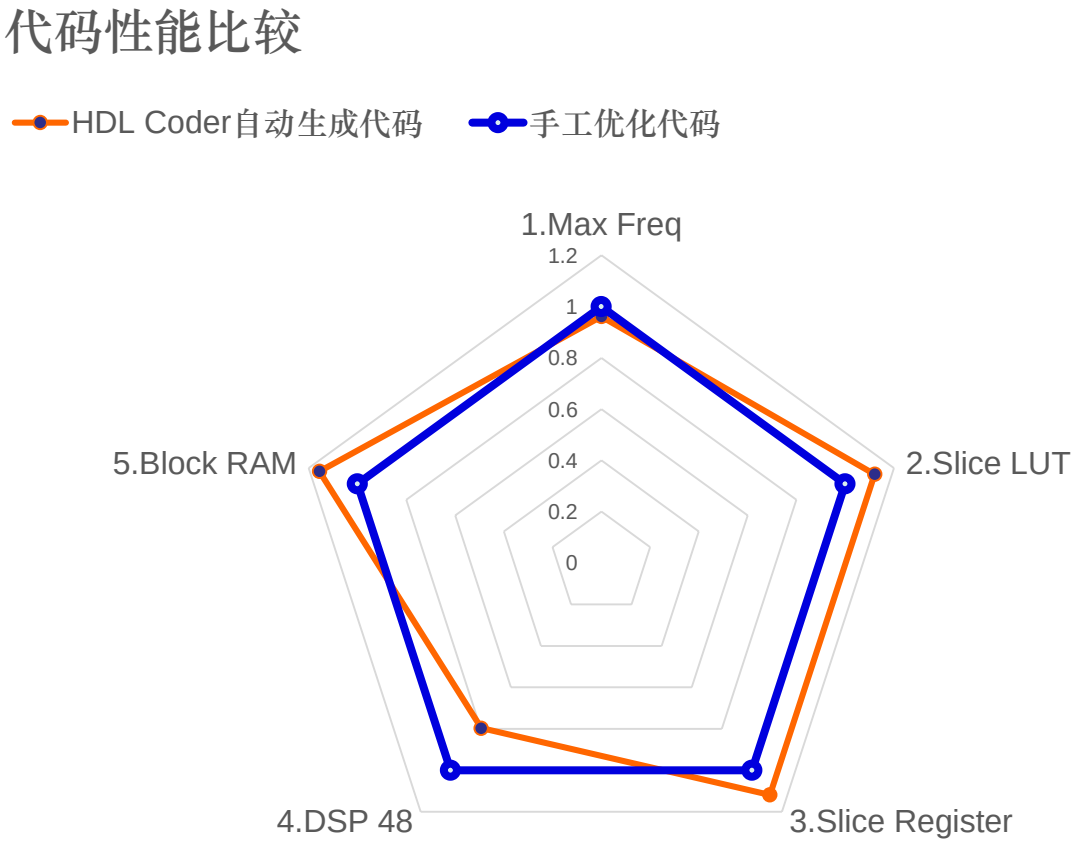
1 功能、性能指标测试



- 近4万行HDL代码，千万门电路规模。
- 功能及电性能指标完全满足要求！

四、MATLAB应用实效

2 代码性能



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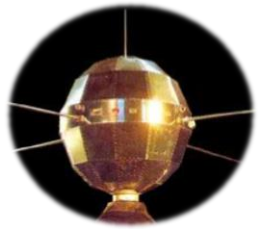

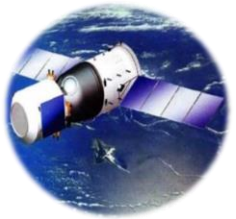

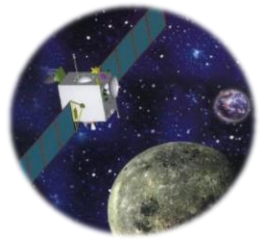

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五、经验和总结

1 设计阶段

01 模型库中模型涵盖广泛

02 提高抽象级

03 模型结构直观，便于查看

04 多测试手段，仿真便利

五、经验和总结

2 实现阶段

01 自动生成代码性能优异

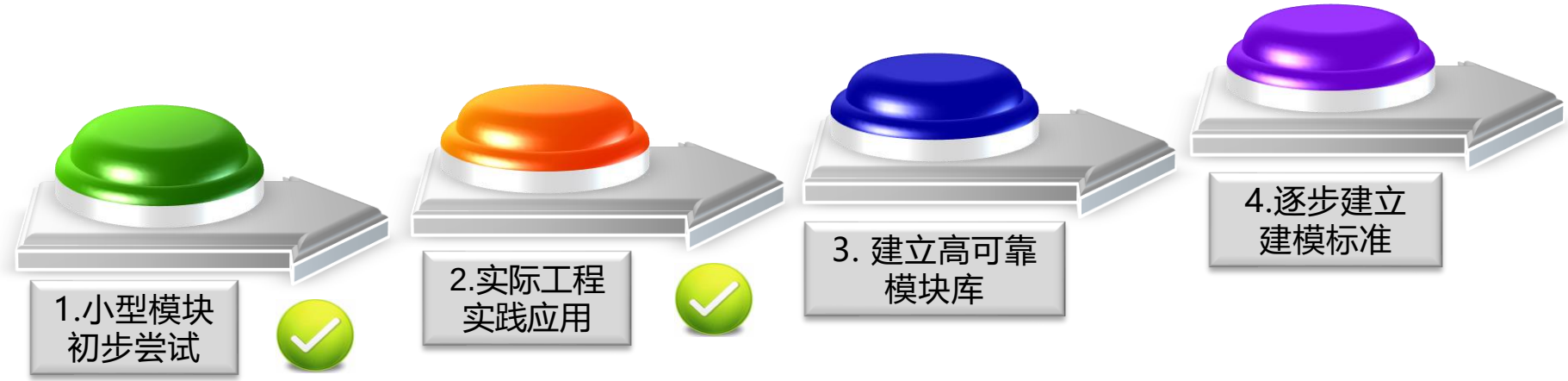
02 加快迭代周期

03 模型复用程度高

04 降低纠错成本

五、经验和总结

3 后续计划



谢 谢!