

MATLAB EXPO

从架构到实现：数学物理建模在Intel Xeon 平台时钟设计的应用

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Agenda

Intel Clock Jitter Analysis Tool

- Background and Design Target
- Comments from Industry: First one to Fix Bottleneck Issues

General Methodological for Applicable Innovation

- Deduction: from Theory to Simulation
- Induction: from Validation to General Methodology
- MathWorks Tools: Combine both to Fix Gaps between Simulation and Validation

A Bigger Picture for Applicable Innovation

- Architecture Level Influence

The background features a complex, abstract pattern of glowing blue and purple particles and light trails, creating a sense of depth and movement. The particles are concentrated in the center, forming a dense, starburst-like shape that tapers towards the edges. The overall color palette is dominated by deep blues and purples, with some lighter, cyan-colored highlights.

Intel Clock Jitter Analysis Tool

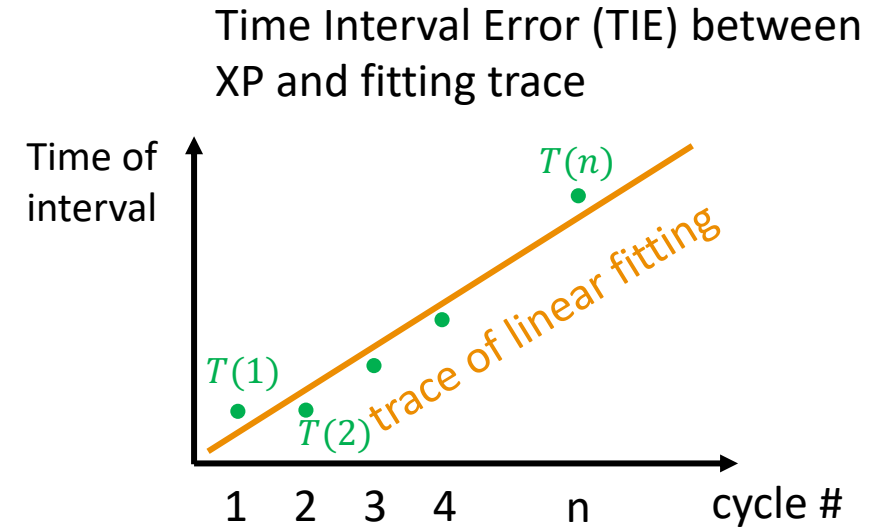
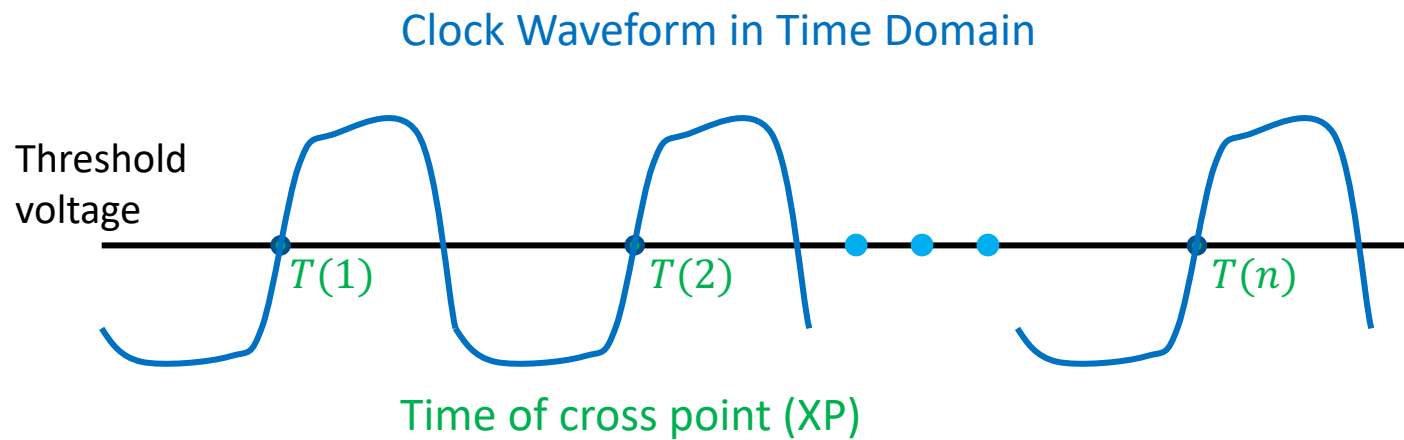
Intel Clock Jitter Analysis Tool (CJAT)

The screenshot displays the Intel Clock Jitter Analysis Tool (CJAT) 0.93 interface, which is divided into several functional areas:

- Configuration Panel (Left):** Contains settings for Generation (PCIe 5.0 DB2000), Clock Mode (Common reflck), DB Topology, Post Process options (Midbus, SSC Removal, NF De-embed, Low Pass Filter), and Crosstalk settings.
- Block Diagram (Top Right):** Illustrates the signal path for Channel A and Channel B. Channel A includes a Clock Source, two DB buffers, and Device A. Channel B includes a Clock Source, a DB buffer, and Device B. Signal paths are labeled with numbers like 1.1, 2.1, 3.1, 4.1, and 7.1.
- Configuration Log (Bottom Left):** Provides a detailed list of system parameters, including Generation, Clock Mode, Transport Delay Spec, Low Pass Filter status, Midbus status, SSC Removal status, System Max Transport Delay (12ns), data direction (both A and B), DB Setting (0 shared, 2 for Channel A, 0 for Channel B), and file paths for clock and noise floor waveforms.
- Test Log (Bottom Right):** Shows the execution status of the analysis, including "Ready", "Configuring...", "Configuration Done", "System level information delivered to process algorithm", "Clock waveform analysis Start", "Base frequency is 99.835 MHz", "Checking Midbus Algorithm for reflection removal...", "Midbus function turned on; New threshold voltage as -0.221 V", "Swing is 0.812 V", "Additional FIR lowpass filter Enabled; Bandwidth as 1.884 GHz", "Clock Period jitter is Delivered", "Clock Period jitter --> Phase jitter WIP...", "Clock Input Phase jitter Delivered", "Clock waveform analysis Done; CDR output Phase jitter Start", "Analyzing input phase jitter pass through all combinations of transfer functions...", "Transfer Functions Generated; Total 16 combinations", "FFT Start; Phase spectrum is generating...", "Sweeping all 16 combinations...", and "FFT Done; Back to Time Domain".

CJAT Background

What is phase jitter/ TIE in clock design?

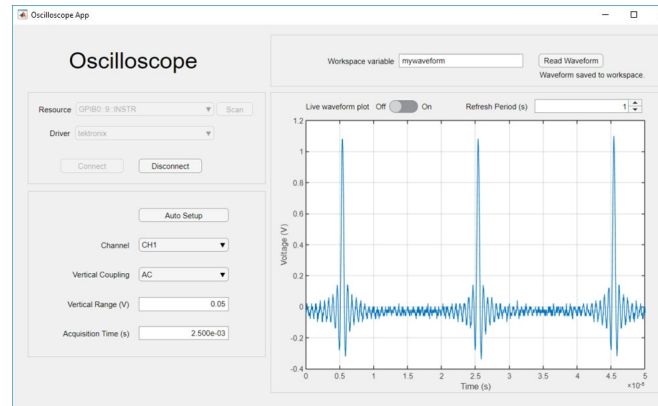
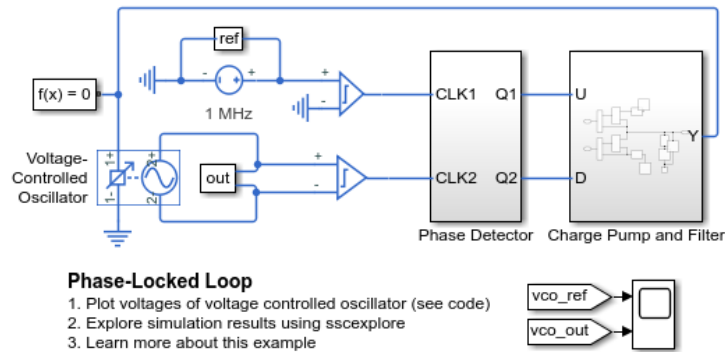


What is the design target?

- More accurate clocking can support higher speed data transfer.
- Take PCIe* 5.0 (32Gbps) as example, phase jitter of clock should <150 fs RMS (~ 2.1 ps pk-pk jitter for BER -12)
- In 2.1 ps, the light travels 0.63 mm ($= 3e8$ m/s * 2.1 ps)

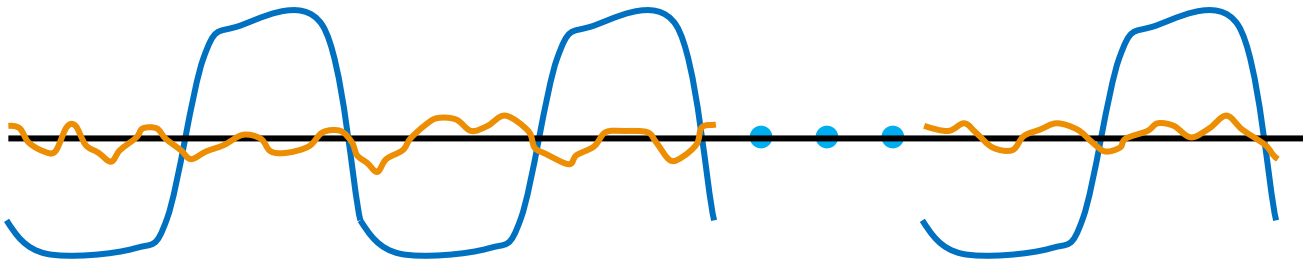
CJAT Background (one feature as example)

Why CJAT is important to industry?



Real phase jitter from clock generator silicon

Jitter from test environment (Noise floor from oscilloscope & probes)



The real phase jitter from silicon is overwhelmed by the impact from oscilloscope & probe noise floor

→ Fail PCIe* limitation

CJAT can remove impact from oscilloscope & probe noise floor and keep real silicon jitter behavior

Post Process	12 ns Spec Default <input checked="" type="checkbox"/> Enable	Low Pass Filter <input checked="" type="checkbox"/> Enable
Midbus <input checked="" type="checkbox"/> Enable	SSC Removal <input checked="" type="checkbox"/> Enable	NF De-embed <input checked="" type="checkbox"/> Enable

The background features a complex, abstract pattern of glowing particles and lines. The particles are small, multi-colored dots in shades of blue, purple, and cyan, scattered across the dark background. The lines are thin, curved, and multi-colored, creating a sense of motion and depth. The overall effect is reminiscent of a starburst or a nebula, with a bright central point from which the particles and lines radiate outwards.

General Methodological for Applicable Innovation

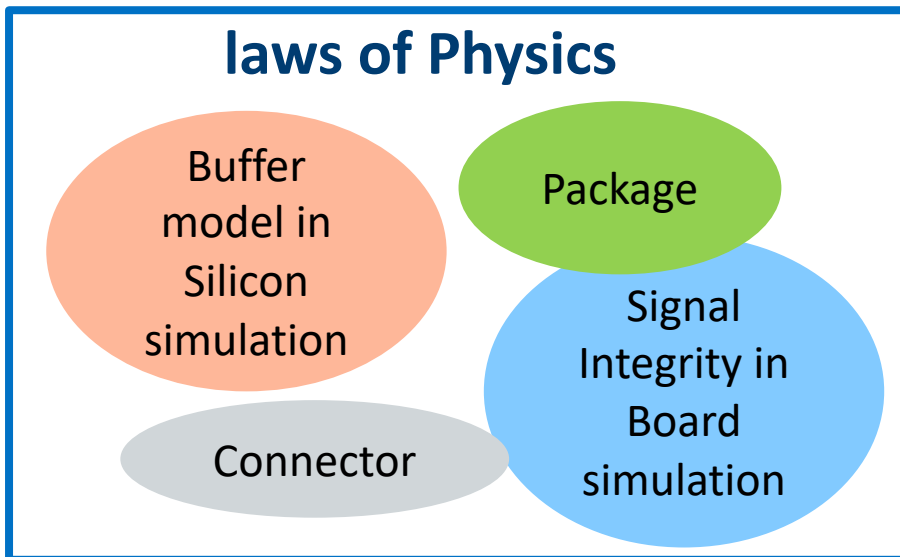
Deduction: from Theory to Simulation

Deduction (logic):

“A process of reasoning that moves from the general to the specific, in which a conclusion follows necessarily from the premises presented, so that the conclusion cannot be false if the premises are true.”

$$P(B|A) = \frac{P(AB)}{P(A)} = 1 \rightarrow A \text{ is part of } B$$

-- Wiktionary



PROs

- Correct when theory is well leveraged

CONs

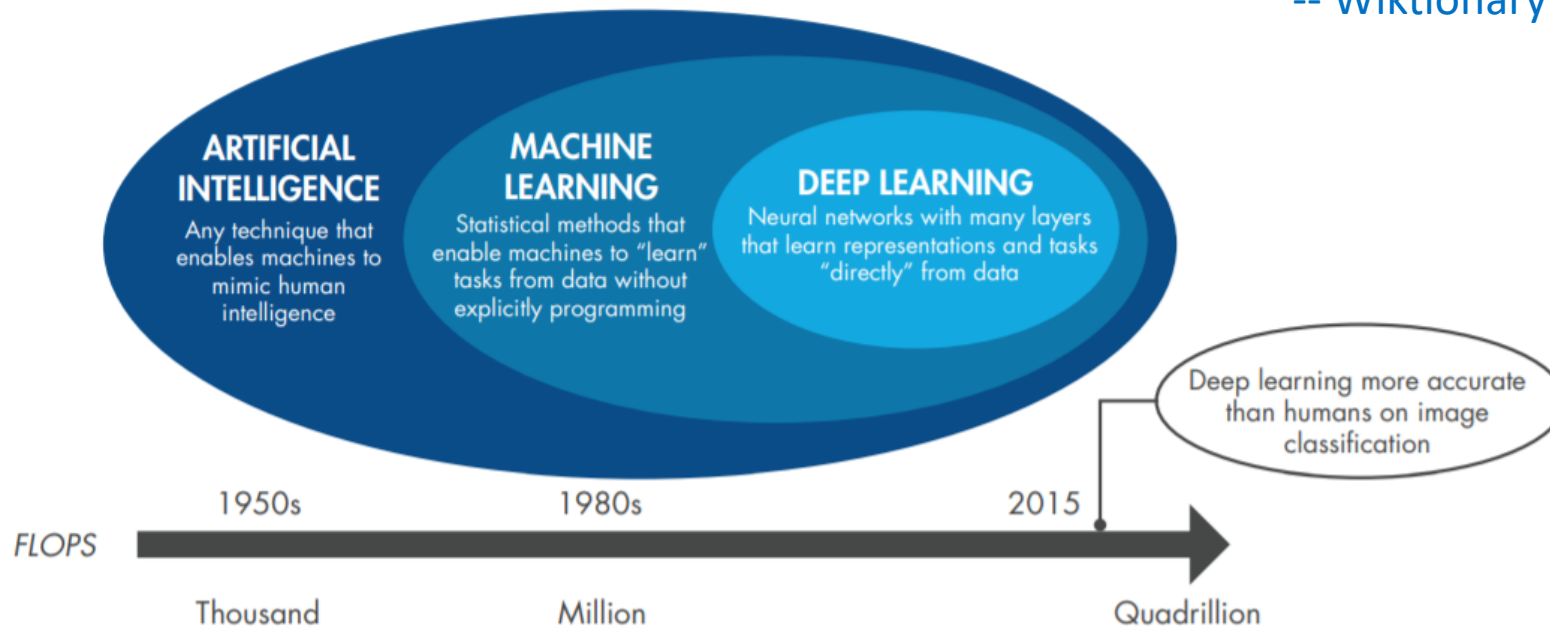
- Not easy for innovation
- Poor correlation between simulation and reality if the theory is over ideal and hard to match

Induction: from Validation to General Methodology

Induction (logic):

“Derivation of general principles from specific instances.”

-- Wiktionary



PROs

- Human nature; easy to use

CONs

- Mistake by poor cognitive ability
- Heavy loading and low efficiency to sweep all corner cases
- “Black Swan”

MathWorks Tools: Combine both

Physics:
from silicon thermal
noise, PLL/ CDR
transfer functions, to
buffer jitter

Deduction

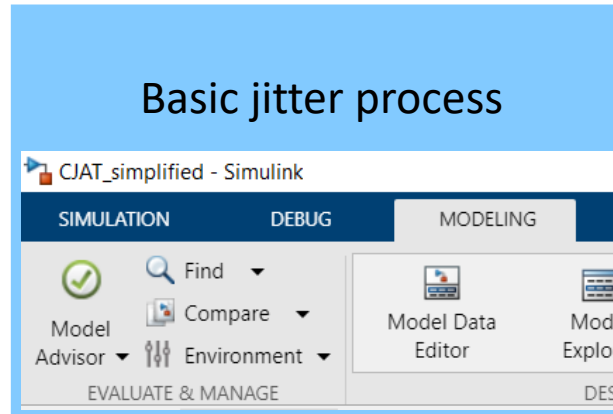
**Mathematics &
Statistics:**
validation sweep with
equipment

Induction

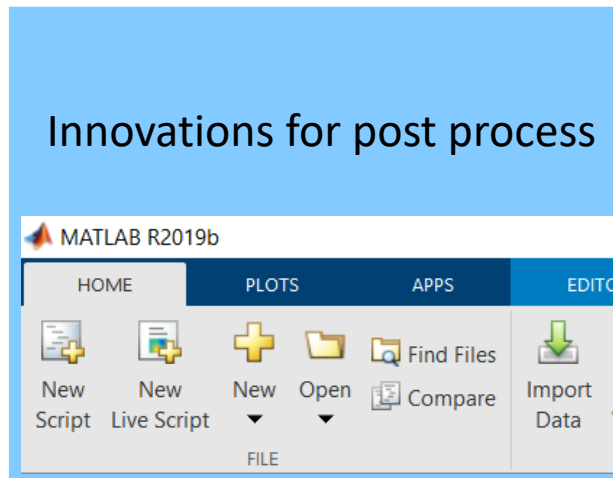
Physics:
pick critical impactors
from noise floor

Deduction

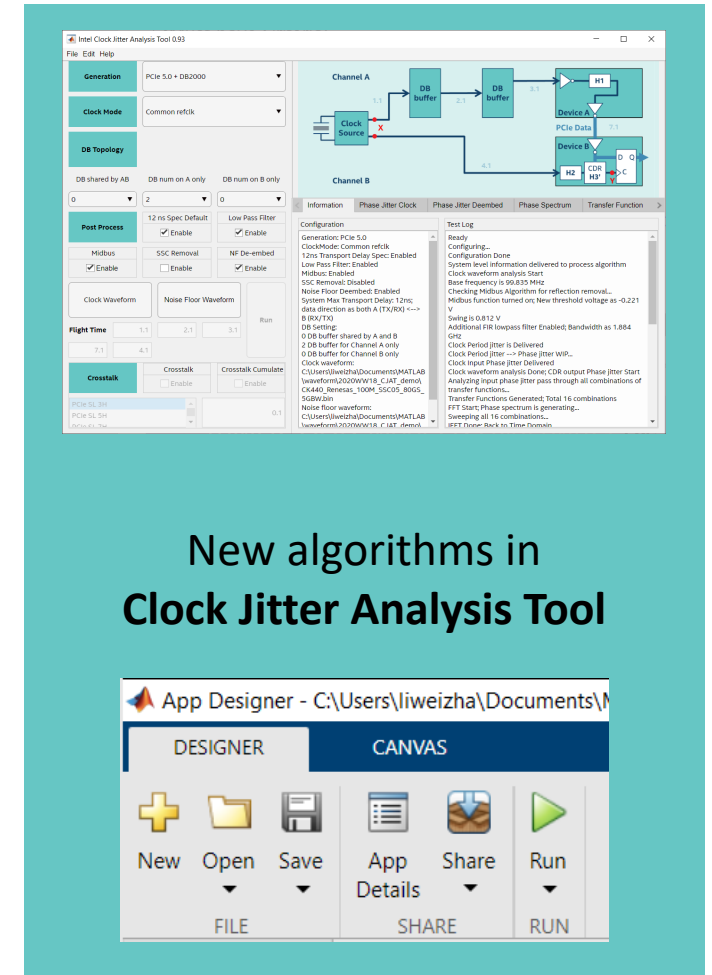
Basic jitter process



Innovations for post process



New algorithms in Clock Jitter Analysis Tool

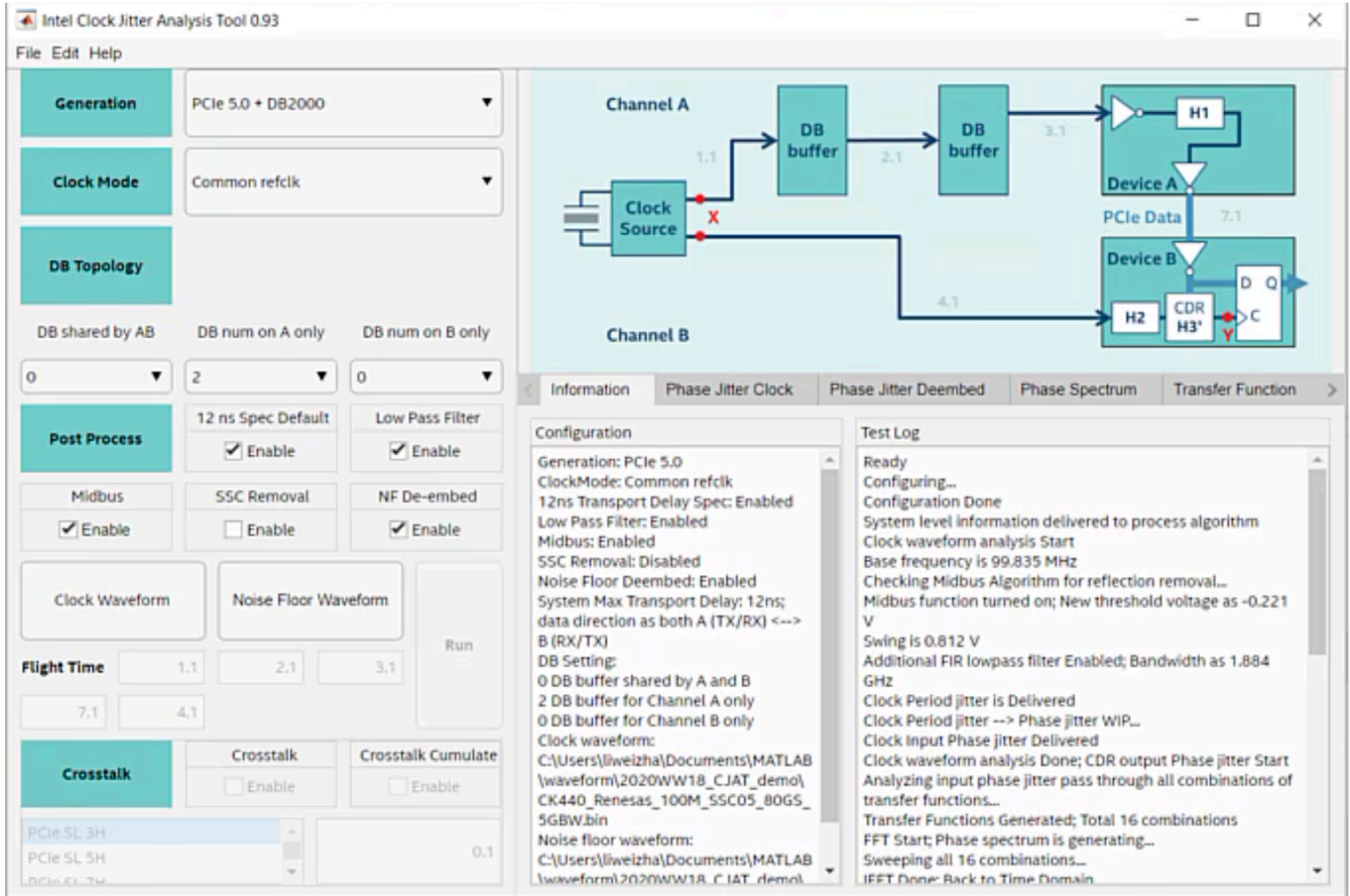


What we used in this tool

MATLAB

- MATLAB Coder
- Optimization Toolbox
- Partial Differential Equation Toolbox
- SerDes Toolbox
- Signal Processing Toolbox
- MATLAB Compiler
- App Designer

Simulink



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A Bigger Picture for Applicable Innovation

Comments from Industry: First to Fix Bottleneck Issues

“By applying solid understanding of high speed theories and signal integrity knowledge to the cutting edge designs, CJAT led the innovation of clock jitters' methodology. Furthermore, by sharing the new algorithms to industry partners, CJAT promoted the state-of-art of the ecosystem and measurement.”

-- Keysight

“With the CJAT, all clock IC vendors can use the program to get the real IC jitter performance. This creates a better way to make sure the clock device can meet the requirements of the Intel chips.”

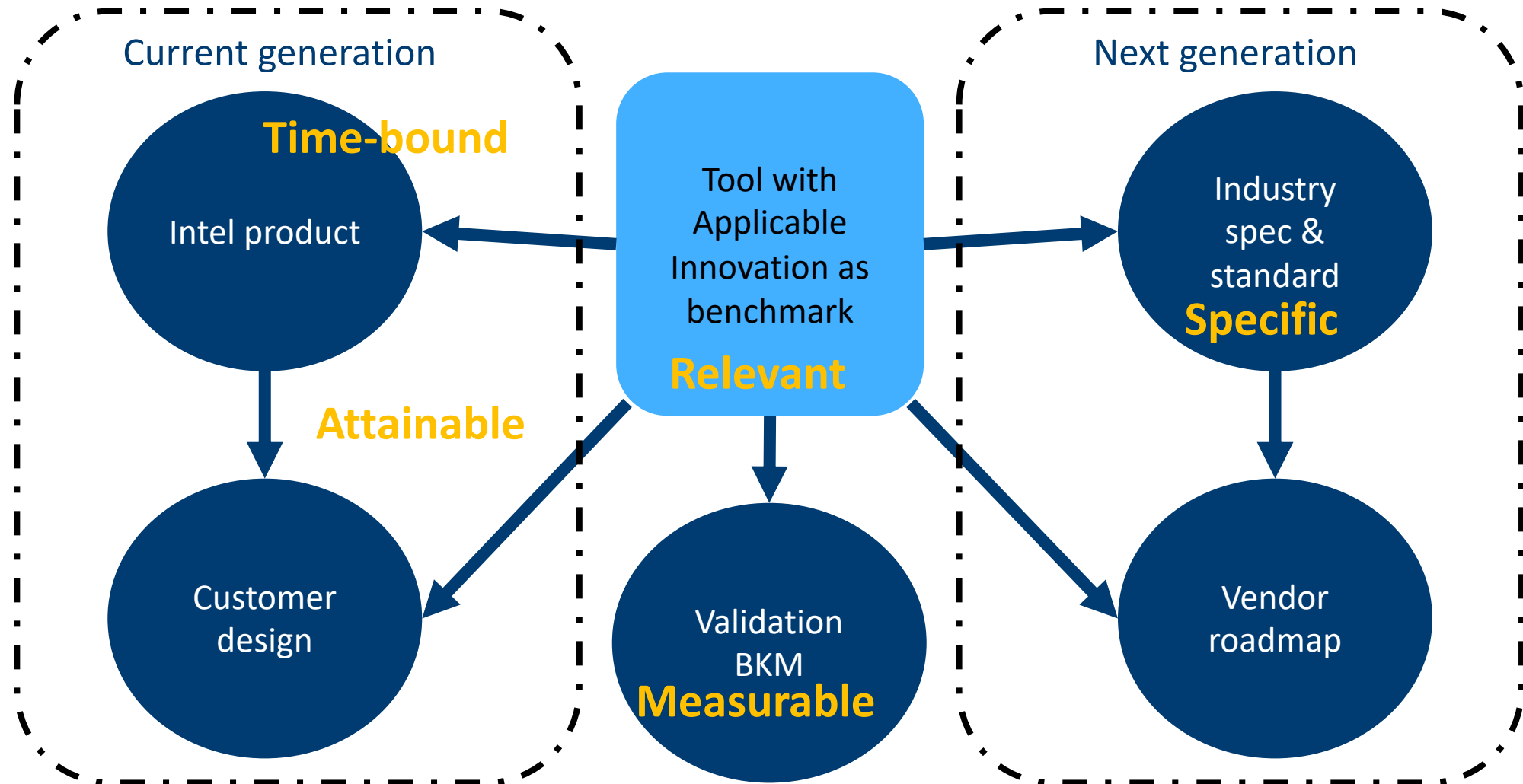
-- Diodes

“Clock distribution is one of hot topics in our Eagle Stream 4S/8S platform design. CJAT is efficient to design/evaluate for our clock solutions. Appreciate it of you for latest released CJAT tool. .”

-- Lenovo

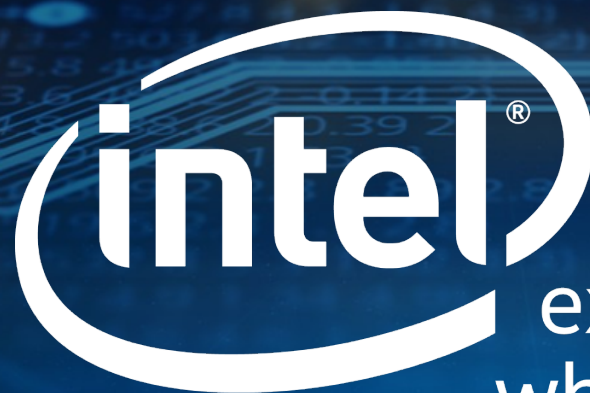
Architecture Level Influence

→ Smart iteration



Q & A





experience
what's inside™