MATLAB EXPO

从架构到实现：数学物理建模在Intel Xeon 平台时钟设计的应用

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MathWorks®

Agenda

Intel Clock Jitter Analysis Tool

- Background and Design Target
- Comments from Industry: First one to Fix Bottleneck Issues

General Methodological for Applicable Innovation

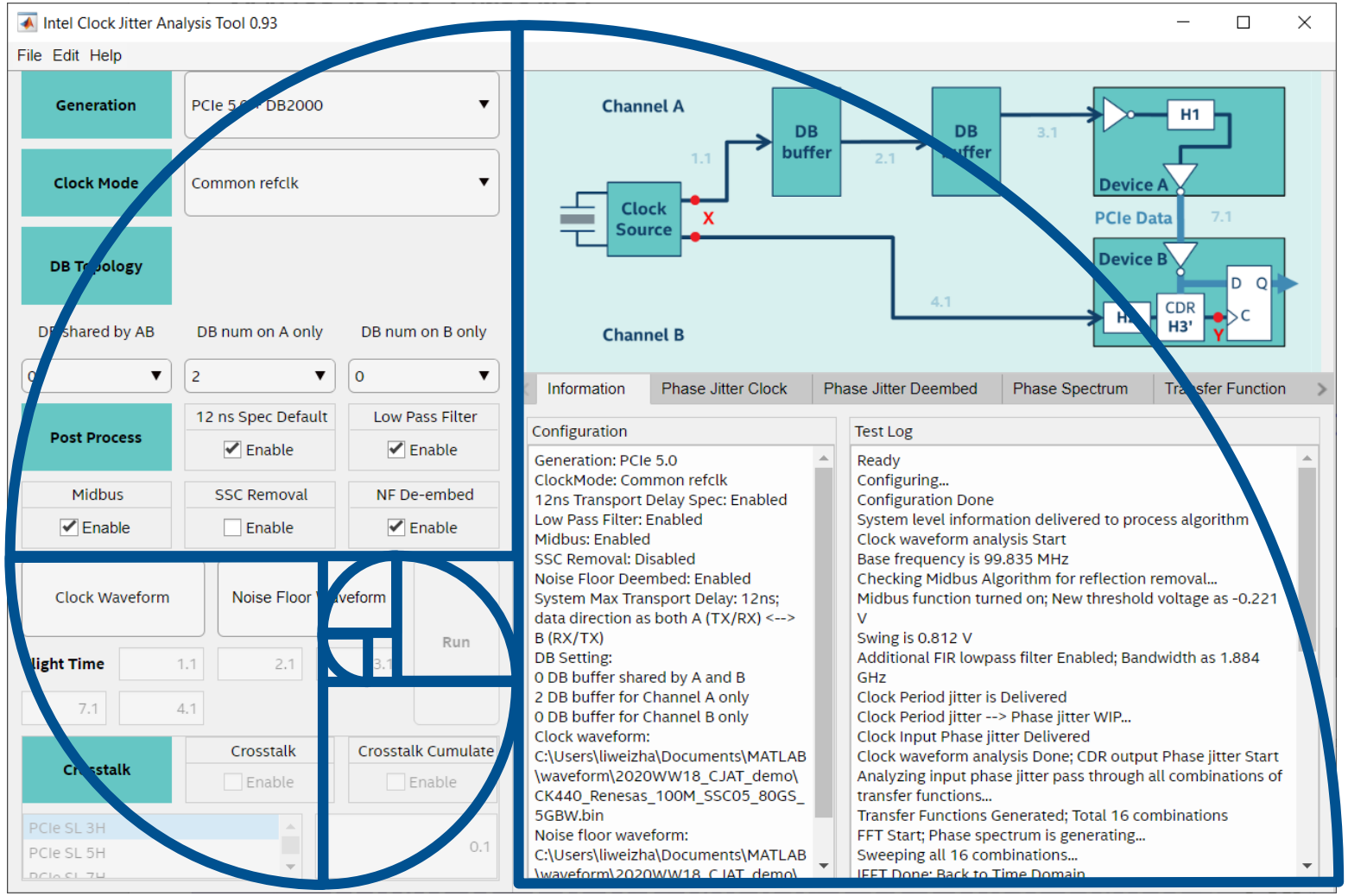
- Deduction: from Theory to Simulation
- Induction: from Validation to General Methodology
- MathWorks Tools: Combine both to Fix Gaps between Simulation and Validation

A Bigger Picture for Applicable Innovation

- Architecture Level Influence

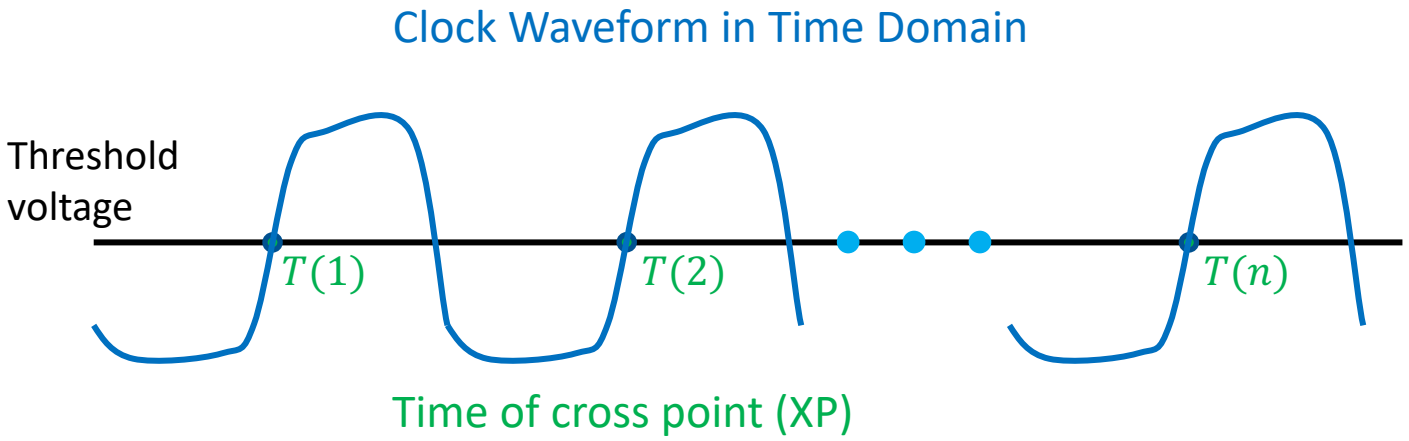

Intel Clock Jitter Analysis Tool

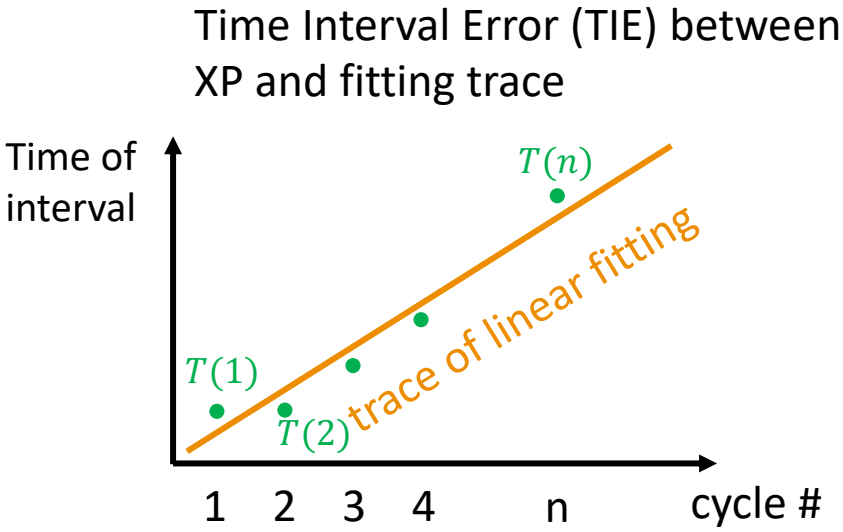
Intel Clock Jitter Analysis Tool (CJAT)



CJAT Background

What is phase jitter/ TIE in clock design?



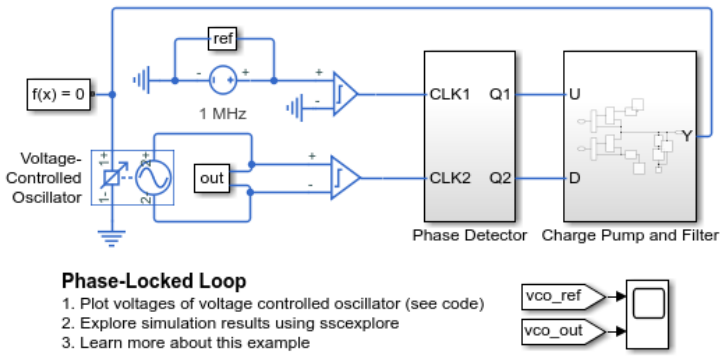


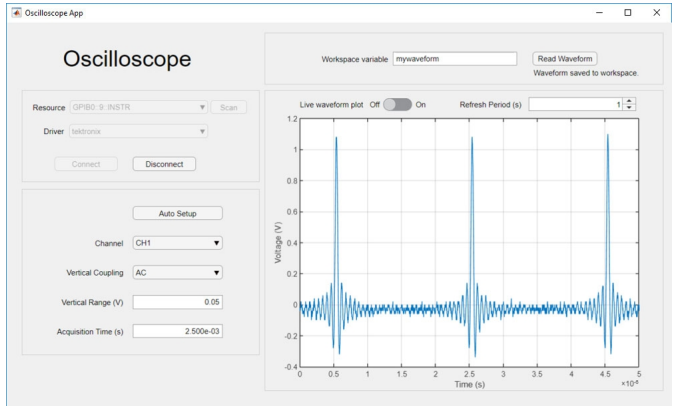
What is the design target?

- More accurate clocking can support higher speed data transfer.
- Take PCIe* 5.0 (32Gbps) as example, phase jitter of clock should <150 fs RMS (~ 2.1 ps pk-pk jitter for BER -12)
- In 2.1 ps, the light travels 0.63 mm (= 3e8 m/s * 2.1 ps)

CJAT Background (one feature as example)

Why CJAT is important to industry?





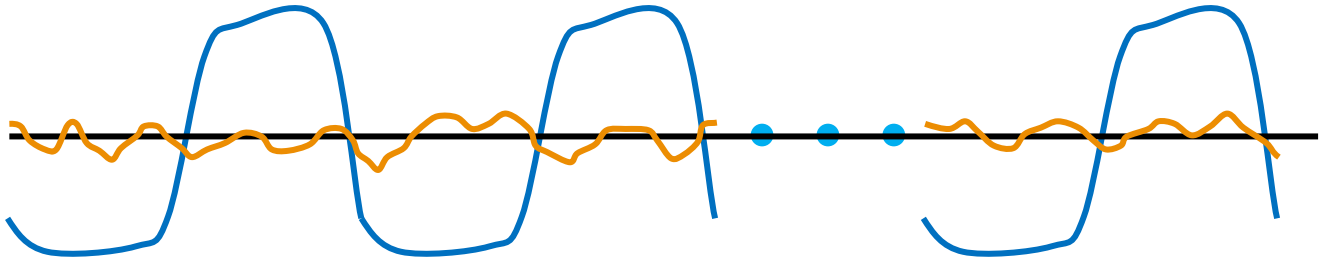
The real phase jitter from silicon is overwhelmed by the impact from oscilloscope & probe noise floor

→ Fail PCIe* limitation

CJAT can remove impact from oscilloscope & probe noise floor and keep real silicon jitter behavior

Real phase jitter from clock generator silicon

Jitter from test environment (Noise floor from oscilloscope & probes)



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General Methodological for Applicable Innovation

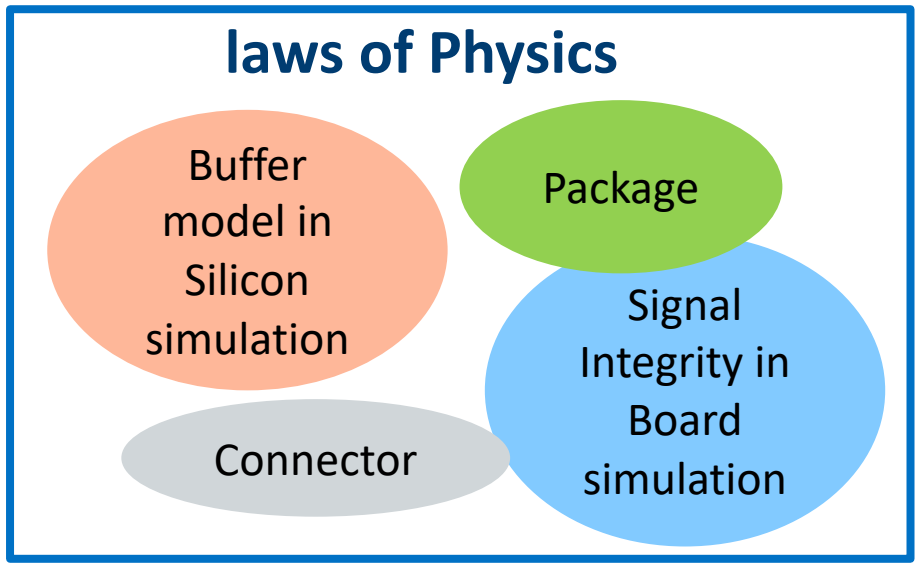
Deduction: from Theory to Simulation

Deduction (logic):

"A process of reasoning that moves from the general to the specific, in which a conclusion follows necessarily from the premises presented, so that the conclusion cannot be false if the premises are true."

-- Wiktionary

$$P(B|A) = \frac{P(AB)}{P(A)} = 1 \rightarrow$$ A is part of B



PROs
- Correct when theory is well leveraged

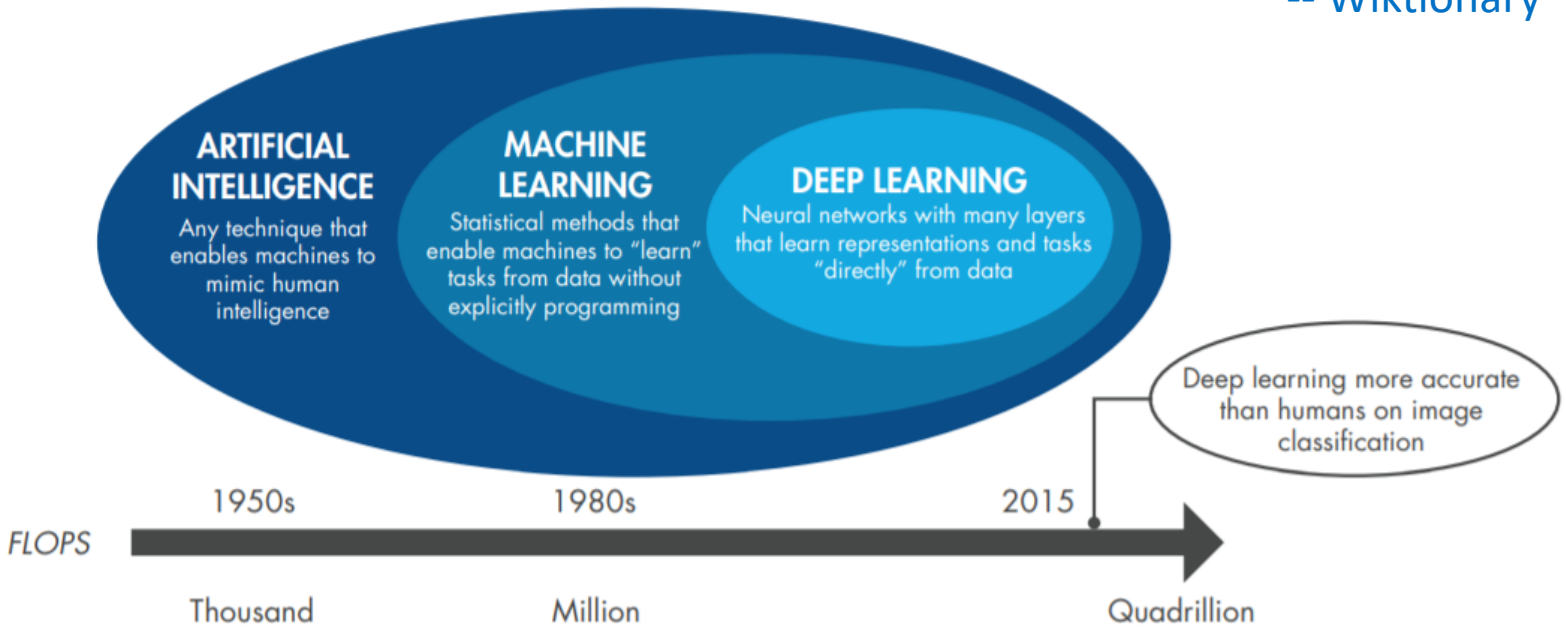
CONs
- Not easy for innovation
- Poor correlation between simulation and reality if the theory is over ideal and hard to match

Induction: from Validation to General Methodology

Induction (logic):

"Derivation of general principles from specific instances."

-- Wiktionary



PROs

- Human nature; easy to use

CONs

- Mistake by poor cognitive ability
- Heavy loading and low efficiency to sweep all corner cases
- "Black Swan"

MathWorks Tools: Combine both

Physics:
from silicon thermal noise, PLL/ CDR transfer functions, to buffer jitter

Deduction

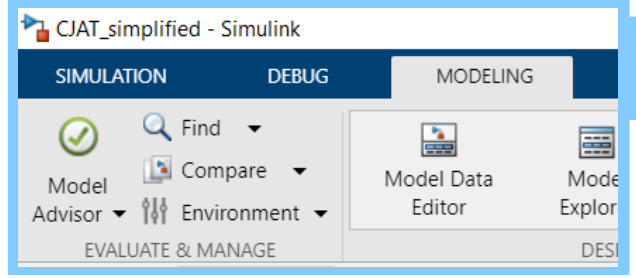
Mathematics & Statistics:
validation sweep with equipment

Induction

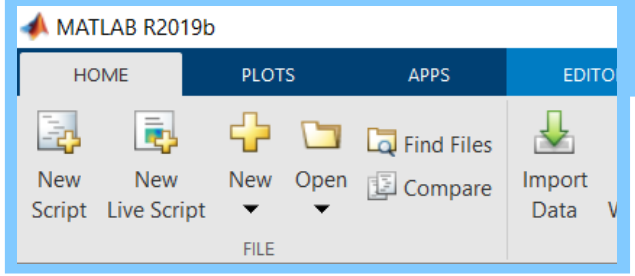
Physics:
pick critical impactors from noise floor

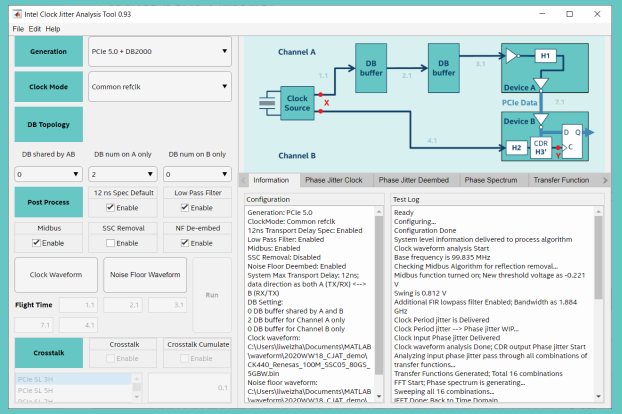
Deduction

Basic jitter process

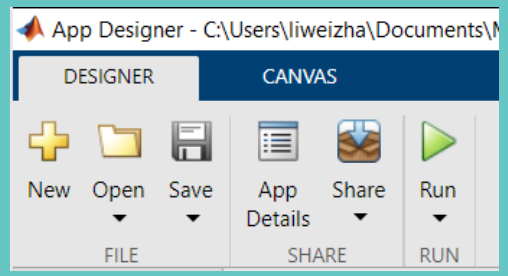


Innovations for post process





New algorithms in
Clock Jitter Analysis Tool

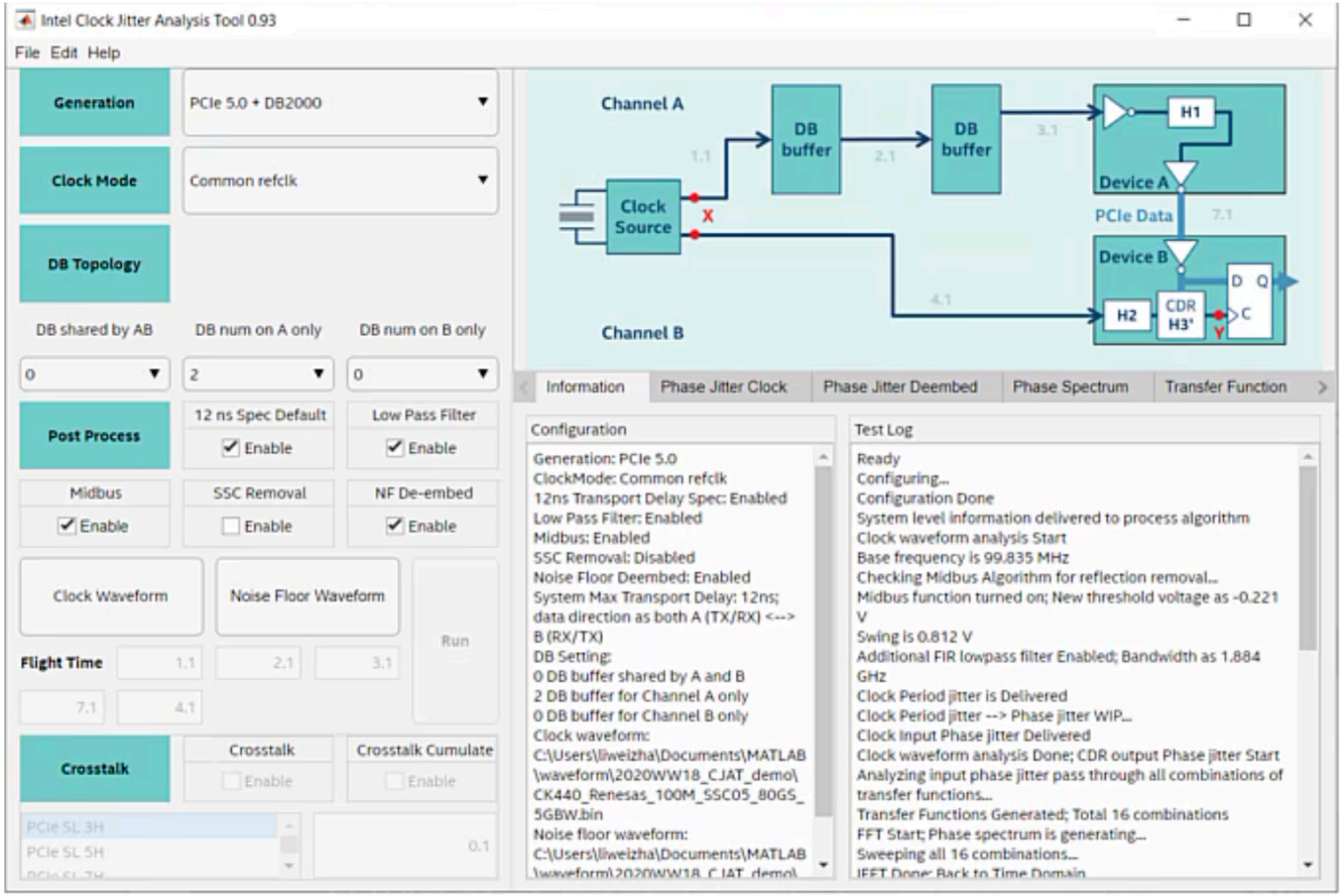


What we used in this tool

MATLAB

- MATLAB Coder
- Optimization Toolbox
- Partial Differential Equation Toolbox
- SerDes Toolbox
- Signal Processing Toolbox
- MATLAB Complier
- App Designer

Simulink




A Bigger Picture for
Applicable Innovation

Comments from Industry: First to Fix Bottleneck Issues

"By applying solid understanding of high speed theories and signal integrity knowledge to the cutting edge designs, CJAT led the innovation of clock jitters' methodology. Furthermore, by sharing the new algorithms to industry partners, CJAT promoted the state-of-art of the ecosystem and measurement."

-- Keysight

"With the CJAT, all clock IC vendors can use the program to get the real IC jitter performance. This creates a better way to make sure the clock device can meet the requirements of the Intel chips."

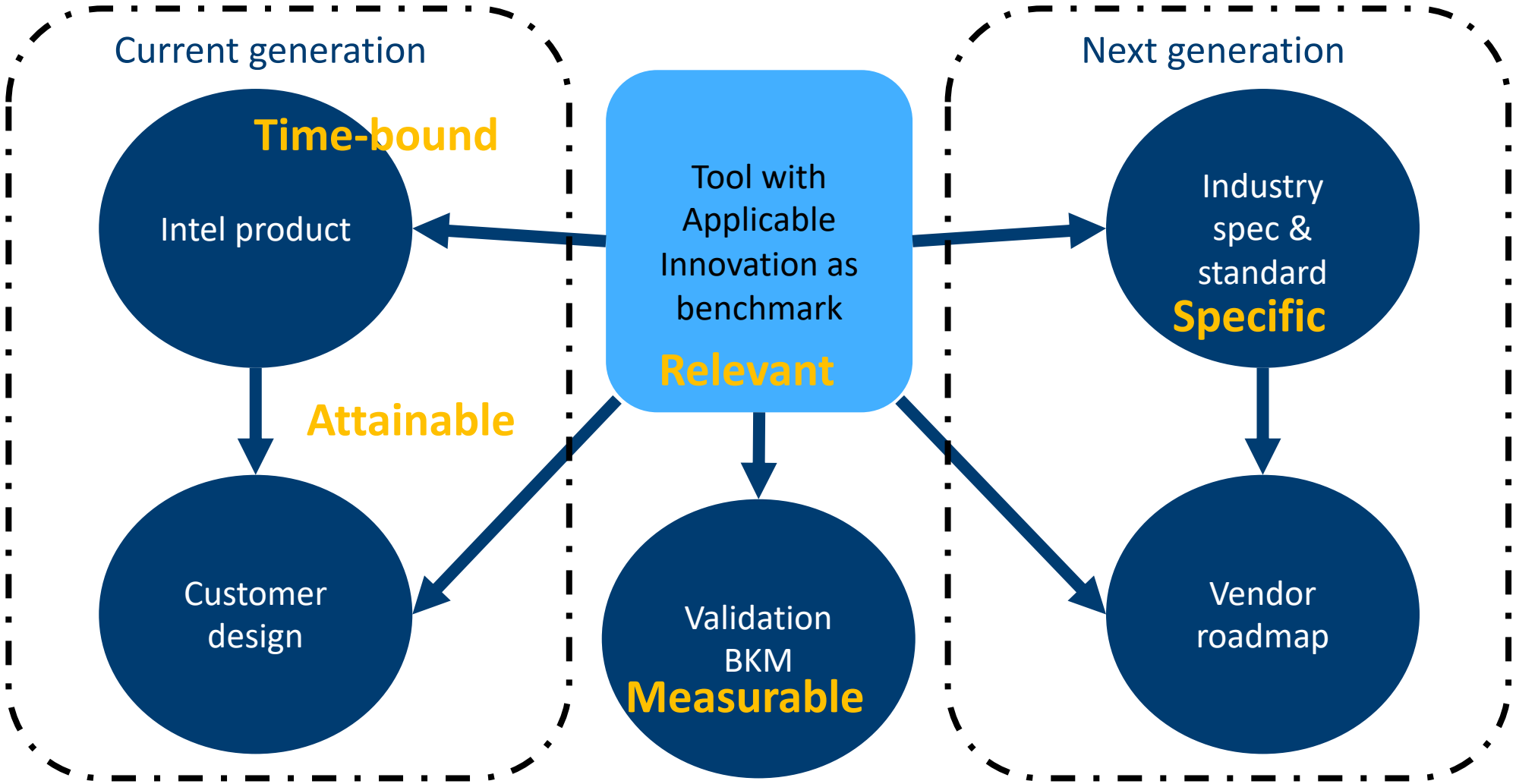
-- Diodes

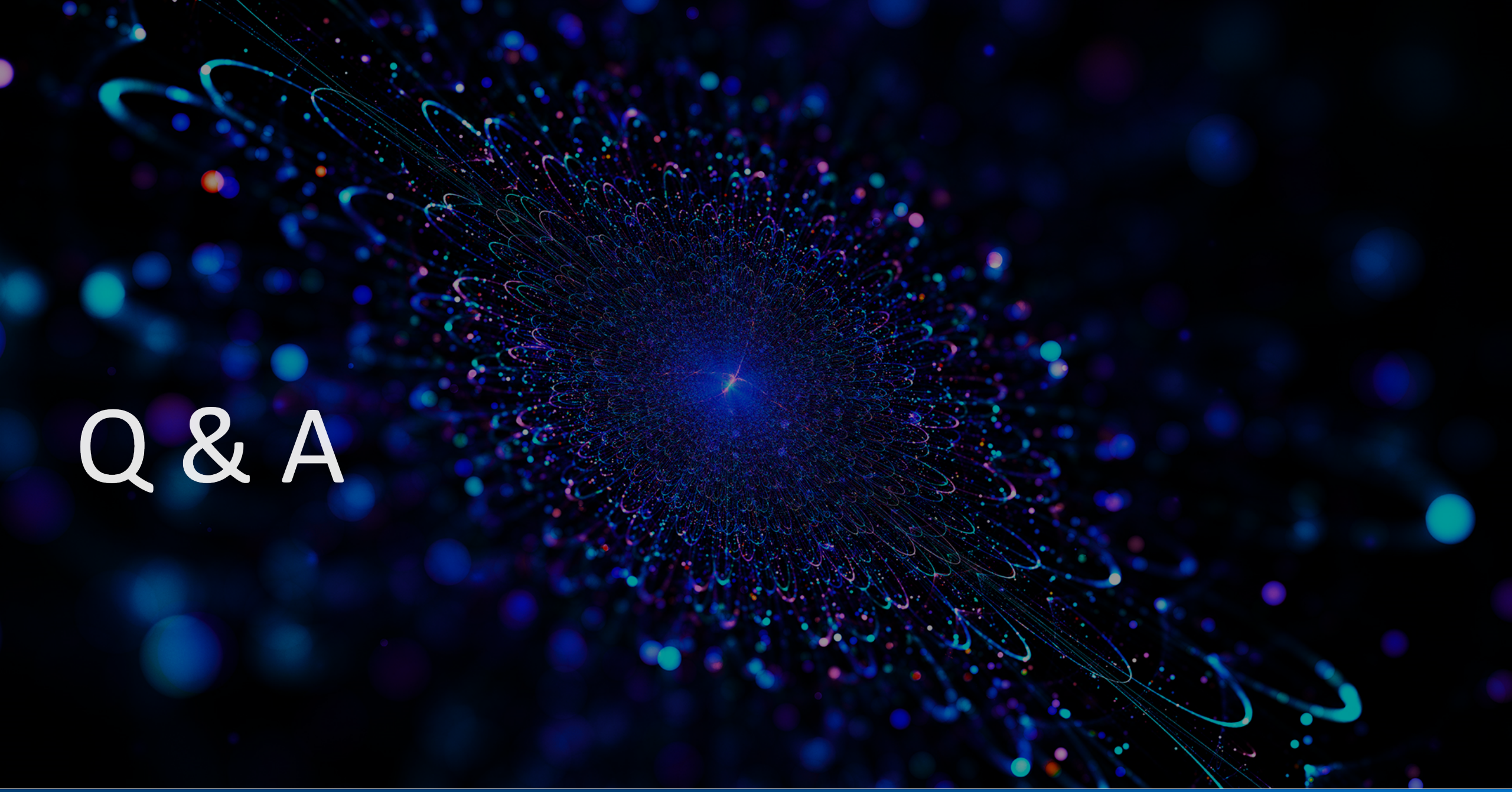
"Clock distribution is one of hot topics in our Eagle Stream 4S/8S platform design. CJAT is efficient to design/evaluate for our clock solutions. Appreciate it of you for latest released CJAT tool. ."

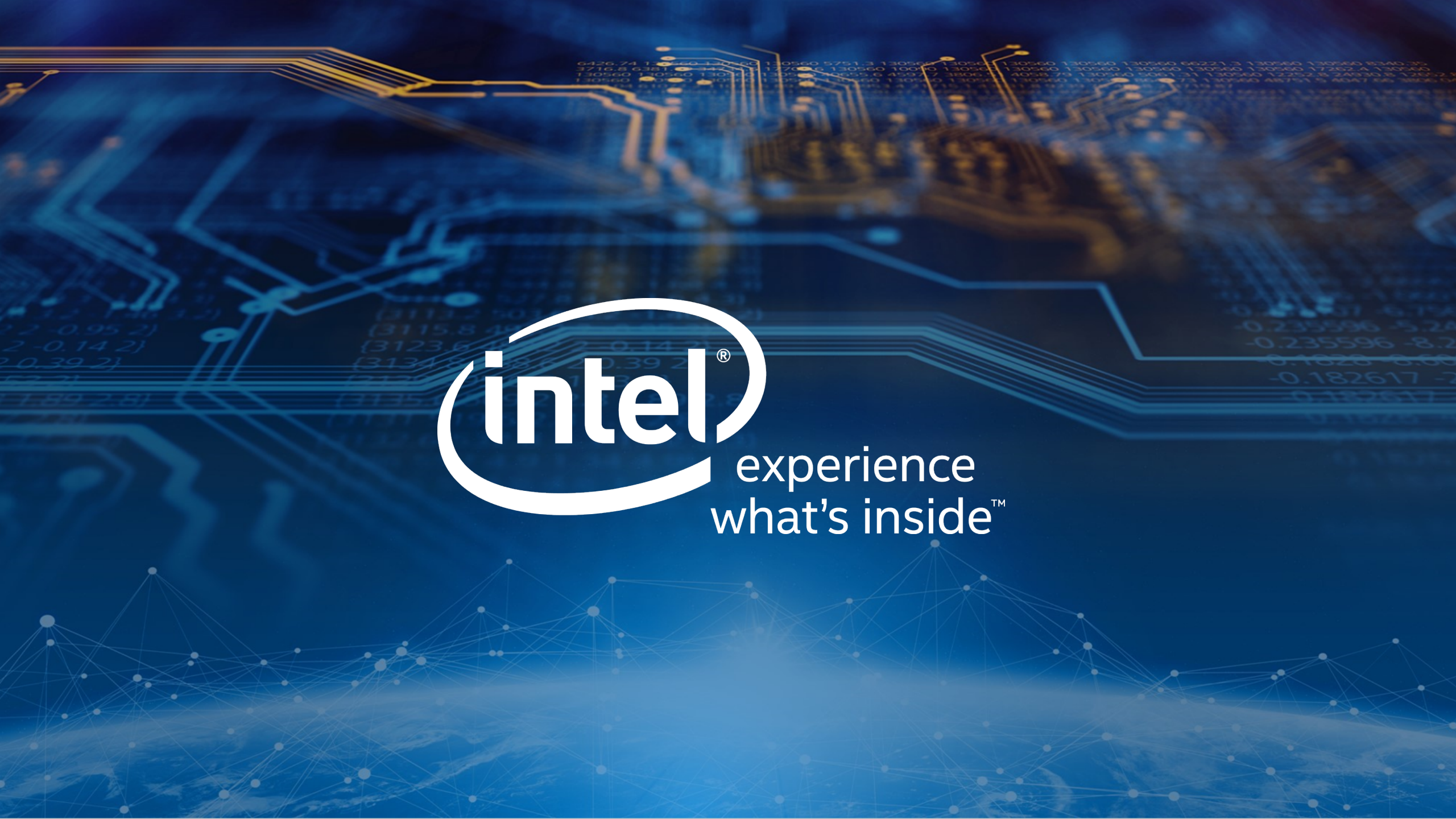
-- Lenovo

Architecture Level Influence

→ Smart iteration




Q & A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